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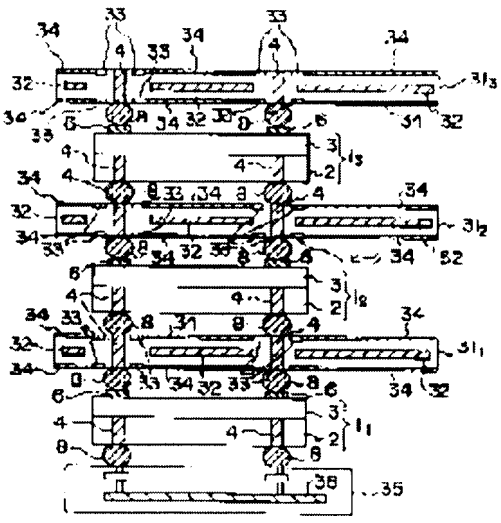
(54) MULTI-CHIP SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a multi-chip semiconductor device whose planar area is small and which is superior in a heat dissipating property.
SOLUTION: A multi-chip semiconductor device is constituted by laminating respective chips 11, 12, 13 provided with silicon substrates 2 on which elements are integrated and formed. A connecting substrate 311 on which conductive plugs 4 are formed inside respective through-holes is installed between the two upper and lower adjacent chips 11, 12. The chips 11, 12 are connected electrically to each other via conductive plugs 4. A metal plate 32 whose thermal conductivity is larger than that of the connecting substrate 311 is installed inside the connecting substrate 311 in order to improve the heat dissipating property of the chips 11, 12. For the chips 12, 13, the chips 12, 13 are connected with similar technique, and the heat dissipating property of the chips 12, 13 is improved.



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CLAIMS

[Claim(s)]
[Claim 1]Two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A multichip semiconductor device, wherein it electrically connected mutually via a connection substrate provided among these and a conductive plug which a breakthrough was formed in said semiconductor substrate and formed in this breakthrough has connected with said connection substrate.
[Claim 2]Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A multichip semiconductor device which a connection substrate by which a conductive plug was formed in a breakthrough is provided, electrically connects said two chips mutually via said conductive plug, and is characterized by said connection substrate having heat dissipation nature higher than said chip.
[Claim 3]The multichip semiconductor device according to claim 1 or 2, wherein a substance in which heat dissipation nature becomes high rather than said chip in said connection substrate is chosen as a component of said connection substrate.
[Claim 4]The multichip semiconductor device according to claim 1 or 2, wherein said connection substrate comprises a connection substrate main part in which said conductive plug was formed, and a high temperature conductivity member whose thermal conductivity is higher than this connection substrate main part.
[Claim 5]The multichip semiconductor device according to claim 4, wherein said high temperature conductivity members are the conductive plates formed in an inside of said connection substrate main part.
[Claim 6]The multichip semiconductor device according to claim 4, wherein said high temperature conductivity member is the radiation fin provided in the surface of said connection substrate main part.
[Claim 7]Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A multichip semiconductor device, wherein a connection substrate by which a conductive plug was formed in a breakthrough is provided, it electrically connects said two chips to said conductive plug via a vamp, respectively and said connection substrate has an exothermic part.
[Claim 8]The multichip semiconductor device according to claim 7 an exothermic part of each connection substrate being independently controllable.
[Claim 9]The multichip semiconductor device according to claim 7, wherein said exothermic part is formed so that said vamp may be surrounded.
[Claim 10]The multichip semiconductor device according to claim 2 or 7, wherein multilevel

interconnection is formed in said connection substrate.
[Claim 11]The multichip semiconductor device according to claim 2 or 7 which a component of said connection substrate is an insulating material, and is characterized by forming a capacitor which used the 1st capacitor electrode and a ground line as the 2nd capacitor, and with which it used said connection substrate as a capacitor insulating film for a power source wire in said connection substrate.
[Claim 12]Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate in which it comes to form a conductive plug is provided in a breakthrough, and said two chips are electrically mutually connected via said conductive plug, And a multichip semiconductor device, wherein said connection substrate has the coefficient of thermal expansion as it of said semiconductor substrate in which a component of said connection substrate is almost the same more highly [heat dissipation nature] than said chip.
[Claim 13]Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A multichip semiconductor device, wherein a connection substrate which it comes to form a conductive plug in a breakthrough is provided, and in said two chips it electrically connects mutually and a component of said connection substrate has the almost same coefficient of thermal expansion as it of said semiconductor substrate via said conductive plug.
[Claim 14]The multichip semiconductor device according to claim 12 or 13, wherein a difference of a coefficient of thermal expansion of a component of said connection substrate and that of a component of said semiconductor substrate is less than **5.0×10^{-6}.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the multichip semiconductor device which is a semiconductor device which used two or more chips.
[0002]
[Description of the Prior Art]In recent years, many transistors, resistance, etc. are connected to the significant part of a computer or communication equipment so that an electric circuit may be attained, and the large scale integration circuit (chip) integrated and formed on the semiconductor substrate is used abundantly. For this reason, the performance of the whole apparatus is connected as greatly as the performance of a chip simple substance.
[0003]On the other hand, what is called a multichip semiconductor device that planned the performance of the whole apparatus is also proposed using two or more chips. The sectional view of the conventional multichip semiconductor device is shown in drawing 19 - drawing 24.
[0004]Drawing 19 shows the multichip semiconductor device of the type which carries out plane configuration of two or more chips 82 on the wiring board 81 of lamination, for example. 83 show the solder bump among the figure.
[0005]Drawing 20 shows the multichip semiconductor device of the type which makes the surface facing each other (Face to Face), and connects chips.
[0006]Drawing 21 shows the multichip semiconductor device of the type which carries out lamination arrangement of two or more chips 82 using the laminate sheet 84.
[0007]Drawing 22 shows the multichip semiconductor device which used wire bonding as a mounting method.
The pad (un-illustrating) of the Si chip 91 is connected with the leadframe 94 of the laminate sheet 93 by the bonding wire 92.

[0008]Drawing 23 shows the multichip semiconductor device which used TAB (Tape Automated Bonding) as a mounting method.
The pad of the Si chip 91 is connected to the pad (un-illustrating) of the laminate sheet 93 via the solder bump 95 and TAB lead 96.

[0009]In drawing 22 and drawing 23, 97 shows a socket and 98 shows the connector pin.
[0010]Drawing 24 shows the multichip semiconductor device which used the flip chip as a mounting method.
The pad 100 arranged in the shape of a lattice all over the Si chip 91 is connected with the pad 101 similarly arranged in the shape of a lattice all over the laminate sheet 99 via the solder bump 102.

[0011]In drawing 24, 103 shows the adhesives of the epoxy resin system containing a filler, it fills up

with these adhesives 103 between the Si chip 91 and the laminate sheet 99, and they carry out adhesion immobilization of these [91 and 93]. 104,105,107 shows a pad and 106,108 shows the solder bump.

[0012]

[Problem(s) to be Solved by the Invention]However, there are the following problems in these conventional multichip semiconductor devices.

[0013]That is, in order that the conventional multichip semiconductor device of drawing 19 may carry out plane configuration of two or more chips 82, there is a problem that the flat-surface area of a device is large.

[0014]In order that the conventional multichip semiconductor device of drawing 20 may laminate two or more chips 82, there is no problem that the flat-surface area of a device becomes large, but there is a problem that lamination number of sheets is limited to two sheets. The problem of being difficult also has the inspection of a device.

[0015]Since the conventional multichip semiconductor device of drawing 21 can laminate two or more chips 82, Although neither the problem which becomes large, nor the problem that lamination number of sheets is limited to two sheets has the flat-surface area of a device, melting of the vamp 83 on the specific chip 82 cannot be carried out selectively, and there is a problem that repair of the chip 82 is difficult. Although a chip generates heat at the time of operation of a chip, since the heat cannot be missed outside effectively, there is a problem that the operating characteristic of a chip deteriorates or the life of a chip becomes short.

[0016]The conventional multichip semiconductor device of drawing 22 a pad with a narrow pitch of the Si chip 91 integrated highly by the bonding wire 92. In order to connect with the leadframe 94 of the laminate sheet 93, it is necessary to carry out alignment of between forming wiring on the laminate sheet 93, and a chip and a laminate sheet in high accuracy, and connection is becoming difficult.

[0017]In order that the conventional multichip semiconductor device of drawing 22 and drawing 23 may connect laminate sheet 93 comrades using the socket 97 and the connector pin 98, a certain amount of height is needed, and there is a problem that the connection gap at the time of laminating is large, and integration of a lengthwise direction is difficult.

[0018]Although this kind of problem is solvable by using the conventional multichip semiconductor device of drawing 24, there are the following problems in the multichip semiconductor device of drawing 24.

[0019]Since the shape of the solder bump 102 is a hard drum form, when high integration of the Si chip 91 progresses further and the size and the pitch interval of the pad 100,101 contract further, If distance (connecting distances) between the Si chip 91 and the laminate sheet 99 is shortened and the path of the solder bump 102 is not made small, the faulty connection that the solder bump 102 of next doors short-circuits will arise.

[0020]However, since the laminate sheet 99 is formed to the Si chip 91 being formed using a Si substrate using the plastic plate which consists of glass epoxy etc., A coefficient of thermal expansion differs between the Si chip 91 and the laminate sheet 99 mutually, if connecting distances are shortened as the result, heat distortion will arise in the solder bump 102, and fatigue breaking will produce them by the repetition which is a thermal excursion. Heat distortion is so large that connecting distances are short, and a fatigue life becomes short. Therefore, the reliability of connection between the Si chip 91 and the laminate sheet 99 falls, so that connecting distances are short.

[0021]SiO_2 which there is a role which makes such heat distortion small in the adhesives 103 with which it filled up between the Si chip 91 and the laminate sheet 99, therefore can bring both coefficient of thermal expansion close is mixed as a filler.

[0022]Although the size of a filler is about 10-30 micrometers, Since the portion with which the adhesives 103 are not filled up will arise if connecting distances become short, the problem of it

becoming impossible to secure the reliability of connection between the Si chip 91 and the laminate sheet 99, but to also secure the reliability of connection during the up-and-down Si chip 91 as the result arises.
[0023]It is in providing the multichip semiconductor device this invention was made in consideration of the above-mentioned situation, and it becomes the place made into the purpose (the 1st purpose) has a small flat-surface area of a device, and possible to inspect a device easily.
[0024]Other purposes (the 2nd purpose) of this invention have a small flat-surface area of a device, and there is in providing the multichip semiconductor device excellent in heat dissipation nature.
[0025]Other purposes (the 3rd purpose) of this invention have a small flat-surface area of a device, and there is in providing the multichip semiconductor device which can repair easily.
[0026]Other purposes (the 4th purpose) of this invention have a small flat-surface area of a device, and there is in providing the multichip semiconductor device which can secure the reliability of connection during an up-and-down chip.
[0027]
[Means for Solving the Problem][Elements of the Invention] -- a multichip semiconductor device (claim 1) concerning this invention, in order to attain the 1st purpose of an account of a top, In a multichip semiconductor device with which an element carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, Two chips of the adjacent upper and lower sides electrically connected mutually via a connection substrate provided among these, and a conductive plug which a breakthrough was formed in said semiconductor substrate and formed in this breakthrough has connected with said connection substrate.
[0028]Here, a breakthrough may be provided in both two both [one side or] of a semiconductor substrate.
[0029]A multichip semiconductor device (claim 2) applied to this invention in order to attain the 2nd purpose of the above, In a multichip semiconductor device with which an element carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate by which ** was formed between two chips of the adjacent upper and lower sides, and a conductive plug was formed in a breakthrough is provided, said two chips electrically connect mutually via said conductive plug, and said connection substrate is characterized by heat dissipation nature being higher than said chip.
[0030]In the above-mentioned multichip semiconductor device (claims 1 and 2), as for other multichip semiconductor devices (claim 3) concerning this invention, a substance in which heat dissipation nature becomes high rather than said chip in said connection substrate is chosen as a component of said connection substrate.
[0031]If it is a case of Si chip, specifically, insulating materials, such as SiC and SiN, will be used for a component of a connection substrate.
[0032]Other multichip semiconductor devices (claim 4) concerning this invention, In the above-mentioned multichip semiconductor device (claims 1 and 2), said connection substrate comprises a connection substrate main part in which said conductive plug was formed, and a high temperature conductivity member whose thermal conductivity is higher than this connection substrate main part.

[0033]If a component of a connection substrate is a case of insulating materials, such as SiC, specifically, a member which comprised metallic materials, such as W and Cu, will be used for a high temperature conductivity member.
[0034]Other multichip semiconductor devices (claim 5) concerning this invention are characterized by said high temperature conductivity members being the conductive plates formed in an inside of said connection substrate main part in the above-mentioned multichip semiconductor device (claim 4).
[0035]Here, conductive plates may be provided on the surface of a connection substrate.

Conductive plates may be provided in both an inside of a connection substrate, and the surface.
[0036]Other multichip semiconductor devices (claim 6) concerning this invention are characterized by said high temperature conductivity member being the radiation fin provided in the surface of said connection substrate main part in the above-mentioned multichip semiconductor device (claim 4).
[0037]Here, a radiation fin may be provided in all the connection substrates, or it may provide in a specific connection substrate, for example, a low connection substrate of heat dissipation nature.
[0038]A multichip semiconductor device (claim 7) applied to this invention in order to attain the 3rd purpose of the above, In a multichip semiconductor device with which an element carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate by which ** was formed between two chips of the adjacent upper and lower sides, and a conductive plug was formed in a breakthrough is provided, said two chips electrically connect with said conductive plug via a vamp, respectively, and, as for said connection substrate, it has an exothermic part.
[0039]Other multichip semiconductor devices (claim 8) concerning this invention can control an exothermic part of each connection substrate independently in the above-mentioned multichip semiconductor device (claim 7).
[0040]A multichip semiconductor device (claim 12) applied to this invention in order to attain the 4th purpose of the above, Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate in which it comes to form a conductive plug is provided in a breakthrough, and said two chips are electrically mutually connected via said conductive plug, And as for said connection substrate, a component of said connection substrate has the almost same coefficient of thermal expansion as it of said semiconductor substrate more highly [heat dissipation nature] than said chip.
[0041]Other multichip semiconductor devices (claim 13) applied to this invention in order to attain the 4th purpose of the above, Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate which it comes to form a conductive plug in a breakthrough is provided, and via said conductive plug, it electrically connects mutually and, as for a component of said connection substrate, said two chips have the almost same coefficient of thermal expansion as it of said semiconductor substrate.
[0042][OPERATION] Since two or more chips are laminated according to the 1st this invention (claim 1), unlike the conventional multichip semiconductor device which carries out the plane position of two or more chips, flat-surface area of a device can be made small.
[0043]Since it will become possible to apply an inspecting probe to the above-mentioned conductive plug easily if a chip with which a conductive plug was formed according to the 1st this invention is arranged at the top or the bottom, a device can be inspected easily.
[0044]According to the 2nd this invention (claims 2-6), flat-surface area of a device can be made small for the same reason as the 1st this invention (claim 1).
[0045]According to the 2nd this invention, since heat dissipation nature is higher than a chip, a way of a connection substrate can miss heat of a chip outside effectively via a connection substrate. And degradation of the operating characteristic of a chip and ephemeralization of a chip by a chip generating heat at the time of operation of a chip can be prevented now by improving heat dissipation nature in this way.
[0046]According to the 3rd this invention (claims 7-9), flat-surface area of a device can be made small for the same reason as the 1st this invention (claim 1).
[0047]According to the 3rd this invention, since a poor chip is separable from a connection substrate by fusing a vamp linked to a poor chip by an exothermic part of a connection substrate, a

chip can be repaired easily. Especially in the case of this invention (claim 8), since an exothermic part of each connection substrate is independently controllable, a chip can be repaired more easily.
[0048]According to the 4th this invention (claims 12-14), flat-surface area of a device can be made small for the same reason as the 1st this invention (claim 1).
[0049]Even if it uses a vamp in order to connect a connection substrate and a semiconductor substrate since it of a coefficient of thermal expansion of a component of a connection substrate and a component of a semiconductor substrate is almost equal according to the 4th this invention, heat distortion is hardly produced by a vamp.
[0050]Therefore, even if high integration of a chip progresses further and distance between a chip and a connection substrate becomes short, the reliability of connection between a connection substrate and a semiconductor substrate can be secured, therefore the reliability of connection during an up-and-down chip can be secured.
[0051]Since it of a coefficient of thermal expansion of a component of a connection substrate and a component of a semiconductor substrate is almost equal, in order to bring both coefficient of thermal expansion close, it is not necessary to use adhesives containing a filler.
[0052]Therefore, even if high integration of a chip progresses further and distance between a connection substrate and a semiconductor substrate becomes short, it does not produce, but the reliability of connection between a chip and a connection substrate is in a portion with which adhesives are not filled up by reservation, therefore it can secure the reliability of connection during an up-and-down chip.
[0053]Thermal conductivity and a coefficient of linear expansion of the main substances used for a component of a semiconductor substrate and a component of a connection substrate which are used for a chip are shown in Table 1.
[0054]
[Table 1]

材　料	熱伝導率 λ ($Wm^{-1}K^{-1}$)	線膨張率 α (10^{-6})
シリコン(Si)	150	2.5
ガリウム砒素(GaAs)	50	5.8
二酸化シリコン(SiO_2)	1	0.5
窒化シリコン(Si_3N_4)	2.3	1.5
ベリリア(BeO)	200	6.0
アルミナ(Al_2O_3)	30	6.0
シリコンカーバイド(SiC)	220	3.7
窒化アルミニウム(AlN)	230	4.3
ポリイミド	0.4	45.0
エポキシガラス(プリント基板)	0.3	15.0

[0055]If a component of a connection substrate in this invention is a case where a component of a semiconductor substrate is Si, for example, in respect of relaxation of heat distortion, its Si of the material is the best, but silicon carbide (SiC) whose Si and coefficient of linear expansion are almost equal, and alumimium nitride (AlN) may be sufficient as it. Since thermal conductivity is higher than Si, these are excellent also in respect of heat dissipation nature.
[0056]When a component of a semiconductor substrate used for a chip is a compound semiconductor, in being gallium arsenide (GaAs), for example, GaAs, beryllia (BeO), and alumina (aluminum$_2O_3$) are suitable.
[0057]Although it is dependent on the size of a contact button (pad), and a pitch and the size of a

connection substrate, how many differences of thermal expansion can approve, As for the difference of the coefficient of thermal expansion of the component of a connection substrate, and that of the component of a semiconductor substrate, for reservation of the reliability of connection during the chip made into the purpose of this invention, it is preferred that it is less than **5.0x10 $^{-6}$.

[0058]

[Embodiment of the Invention]Hereafter, an embodiment of the invention (henceforth an embodiment) is described, referring to drawings.

[0059](A 1st embodiment) Drawing 1 is a sectional view of the multichip semiconductor device concerning a 1st embodiment of this invention.

[0060]This multichip semiconductor device has the composition that two chip 1 $_1$ and 1 $_2$ were connected via the laminated wiring board 9 made from ceramics. Chip 1 $_1$ and 1 $_2$ are roughly divided, and comprise the silicon substrate 2 by which accumulation formation of the element was carried out, and the multilayer interconnection layer 3 for connecting an element to a predetermined relation.

[0061]The pad 6 provided in the multilayer interconnection layer 3 of chip $_1$ is electrically connected to the pad 6 provided in the laminated wiring board 9 via the solder bump 8. Other pads 6 provided in the laminated wiring board 9 electrically connected to this pad 6 are electrically connected to the pad 6 provided in the multilayer interconnection layer 3 of chip 1 $_2$. Thus, two up-and-down chip $_1$ and chip 1 $_2$ will electrically be mutually connected via the laminated wiring board 9 formed among these.

[0062]The conductive penetration plug 4 (conductive plug) which penetrates the silicon substrate 2 is formed in chip 1 $_2$. This penetration plug 4 is electrically connected to the pad 6 provided in chip 1 $_2$, and the pad 6 provided in the laminated wiring board 9 via the vamp 8 on it.

[0063]The penetration plug 4 is formed in the outside of an element formation region, and the insulator layer 5 is formed between the penetration plug 4 and the silicon substrate 2 (breakthrough). The connecting plug comprises this insulator layer 5 and the penetration plug 4.

[0064]The silicon field of the silicon substrate 2 of an opposite hand, i.e., fields other than penetration plug 4, is covered with the insulator layer 7 in the multilayer interconnection layer 3 of chip 1 $_2$. There is an effect which promotes heat dissipation in such a penetration plug 4.

[0065]As other means to promote heat dissipation, forming the laminated wiring board 9 with the material whose thermal conductivity is higher than chip 1 $_1$ and 1 $_2$ is raised. If it is a case of Si chip, specifically, insulating materials, such as SiC and SiN, will be raised. A metal plate may also be embedded inside so that a 2nd embodiment may explain.

[0066]Since chip 1 $_2$ is laminated via the laminated wiring board 9 on chip 1 $_1$ according to this embodiment, unlike the conventional multichip semiconductor device which carries out the plane position of two or more chips, flat-surface area of a device can be made small.

[0067]Since chip 1 $_2$ which has the penetration plug 4 which electrically connected with chip 1 $_1$ via the laminated wiring board 9 is used according to this embodiment, a device can be inspected by applying an inspecting probe to the penetration plug 4. Here, since it has exposed to the rear face of the semiconductor substrate 2, the penetration plug 4 can hit an inspecting probe to the penetration plug 4 easily. Therefore, according to this embodiment, it is so that a device can be inspected easily.

[0068]Although the case where a chip was two pieces was explained here, At this embodiment, since chips are connected with the laminated wiring board 9, unlike the conventional multichip semiconductor device which connects chips by Face to Face, there is no problem that the lamination number of sheets of a chip is limited to two sheets.

[0069]Therefore, according to this embodiment, the multichip semiconductor device which the flat-surface area of a device is small, and can inspect a device easily and with which lamination number of sheets is not limited to two sheets can be realized now.
[0070]In this embodiment, although the penetration plug 4 was formed in chip 1_2, it may provide in chip 1_1, or may provide in both chip 1_1 and 1_2.
[0071](A 2nd embodiment) Drawing 2 and drawing 3 are the process sectional views showing the formation method of the penetration plug 4 of the multichip semiconductor device of drawing 1. In the following figures, the above-mentioned figure and identical codes show identical parts or a considerable portion, and detailed explanation is omitted.
[0072]First, as shown in drawing 2 (a), the silicon substrate 2 is prepared. The thing of which stage after the element formation in the middle of element formation may be sufficient as this silicon substrate 2 before isolation and after isolation.
[0073]The substrate after forming before element formation and the STI isolation back in the field enclosed with a round mark among the figure and forming a protective film (BPSG) on a MOS transistor (after element formation) is shown. As after element formation, it is raised, after forming wiring in others.
[0074]As the element formation middle, the next process after forming a required well in a substrate face by an ion implantation, and the next process after forming a gate electrode are raised, for example.
[0075]Next, as shown in drawing 2 (b), after forming the mask pattern 11 with a thickness of 1 micrometer which consists of SiO_2 on the silicon substrate 2, Etching gas etches the silicon substrate 2 selectively by using the mask pattern 11 as a mask using RIE of gas F system, and forms the 100-micrometer-deep slot 12 in the surface of the silicon substrate 2. This slot 12 serves as a breakthrough eventually.
[0076]Here, although the component used the mask pattern 11 of SiO_2 instead, a component may use the mask pattern 11 of the material which has a high selection ratio to Si, such as aluminum and aluminum$_2O_3$.
[0077]The processing technology which forms the slot 12 (breakthrough) is not limited to RIE, and can also use optical etching, wet etching, ultrasonic machining, and an electron discharge method. The above-mentioned processing technology may be combined suitably. The method which combined RIE or optical etching, and wet etching is explained later.
[0078]Next, as shown in drawing 2 (c), after removing the mask pattern 11, use an LPCVD method for the whole surface and a 100-nm-thick SiO_2 film and a 100-nm-thick Si_3N_4 film are deposited on it one by one, The insulator layer 5 of the laminated structure which consists of a SiO_2 film and an Si_3N_4 film is formed. The insulator layer of a monolayer may be used instead of the insulator layer 5 of a laminated structure.
[0079]Next, as shown in drawing 2 (d), the polycrystalline silicon film 4 of low resistance used as a penetration plug in which impurities, such as B, were doped is formed in the whole surface at thickness overflowing from the slot 12, and the inside of the slot 12 is embedded with the polycrystalline silicon film 4.
[0080]As a formation method of the polycrystalline silicon film 4, a CVD method and a sputtering technique are used, for example. Plating can also be used when using a metal membrane instead of the polycrystalline silicon film 4.
[0081]Here, although the polycrystalline silicon film 4 in which the impurity was doped was used as a conductive film used as a penetration plug instead, the amorphous silicon film in which the impurity was doped may be used. Metal, such as W film, a Mo film, a Ni film, and a Ti film, or these metal silicide films may be used.

[0082]Next, the polycrystalline silicon film 4 and the insulator layer 5 are retreated until the surface of the silicon substrate 2 is exposed using methods, such as the CMP method and the etchback method, as shown in drawing 3 (a). As a result, the structure where the polycrystalline silicon film (penetration plug) 4 was embedded via the insulator layer 5 in the slot 12 is formed.
[0083]Next, as shown in drawing 3 (b), the multilayer interconnection layer 3 is formed on the silicon substrate 2 of the side in which the penetration plug 4 was formed. Before forming this multilayer interconnection layer 3, isolation and element formation are performed. Subsequently, the pad 6 is formed in this slot after forming a slot in the surface of this multilayer interconnection layer 3.
[0084]Next, the silicon substrate 2 is retreated until the insulator layer 5 of the pars basilaris ossis occipitalis of the slot 12 exposes the surface (henceforth a rear face) of the silicon substrate 2 of the side and opposite hand in which the penetration plug 4 was formed, as shown in drawing 3 (c). Retreat (thinning) of the silicon substrate 2 is performed by the method which used the processing technology of CMP, chemical polishing, mechanical polishing, wet etching, plasma etching, or vapor etching, or the method which combined these processing technology, for example.
[0085]Next, the rear face of the silicon substrate 2 is selectively etched until the insulator layer 5 of the side attachment wall of the slot 12 above the insulator layer 5 of the pars basilaris ossis occipitalis of the slot 12 is exposed, as shown in drawing 3 (d). CDE, RIE, or wet etching is used for this etching, for example.
[0086]Next, as shown in the figure (d), the insulator layer 7 (the 2nd insulator layer) which consists of SiO_2 is deposited on the rear face of the silicon substrate 2 using plasma CVD method.
[0087]When a low temperature process is required, it is good to use coating films, such as a SOG film, instead of the insulator layer 7 which consists of SiO_2. It is good to make small the stress which the silicon substrate 2 receives to use the insulator layer which consists of organic materials, such as polyimide, instead of SiO_2.
[0088]Next, the penetration plug 4 and the insulator layers 5 and 7 are ground using the CMP method until the rear face of the silicon substrate 2 is exposed, as shown in drawing 3 (e).
[0089]As a result, the structure where the penetration plug (polycrystalline silicon film 4) was embedded at the breakthrough (slot 12), and the silicon field of the rear face of the silicon substrate 2 was covered with the insulator layer 7 is formed.
[0090]As stated above, after forming in the surface of the silicon substrate 2 the slot 12 which does not penetrate this silicon substrate 2, by this embodiment, the structure where the breakthrough (slot 12) was embedded with the penetration plug (polycrystalline silicon film 4) is formed by grinding silicon substrate 2 grade from a rear face.
[0091]Therefore, since according to this embodiment it is not necessary to form a deep breakthrough even if the silicon substrate 2 of a basis is thick (usually thick), the structure where the breakthrough (slot 12) was embedded by the connecting plug (the polycrystalline silicon film 4, the insulator layer 5) can be formed easily.
[0092]With the insulator layer 7, when there is no wrap necessity, a silicon field on the back, At the process of drawing 3 (c), the structure where the breakthrough (slot 12) was embedded by the connecting plug (the polycrystalline silicon film 4, the insulator layer 5) is completed by grinding the silicon substrate 2 and the insulator layer 5 until the polycrystalline silicon film 4 is exposed.
[0093]As for polish (retreat) of the silicon substrate 2, it is preferred to carry out, after starting the silicon substrate 2 from a wafer. It is because a wafer is generally large, and a mechanical strength is weak, so it is difficult to grind uniformly (retreat).
[0094]The sectional view of the connecting plug of various structures is shown in drawing 4. This is a sectional view equivalent to the process of drawing 3 (b). In the figure, the multilayer interconnection layer 3, the pad 6, and the insulator layer 7 are omitted.
[0095]Drawing 4 (a) shows the connecting plug which has the low stress film 13.
[0096]That is, the outside of this connecting plug comprises the conductive film 4a, and the inside

comprises the low stress film 13 in which the difference of a coefficient of thermal expansion with the semiconductor substrate 2a is smaller than the conductive film 4a.

[0097]Any of an insulator layer, semiconductor membrane, and a metal membrane may be sufficient as the low stress film 13. The stress which the silicon substrate 2 receives can be reduced now by using such a connecting plug.

[0098]Like this embodiment, when the component (silicon) of a penetration plug (polycrystalline silicon film 4) and a semiconductor substrate (silicon substrate 2) is the same, such a structure is not necessarily required.

[0099]Drawing 4 (b) shows the connecting plug which has the cap metal membrane 14. That is, the polycrystalline silicon film 4 is not formed only by Mr. Fukashi in the middle of a breakthrough, but the cap metal membrane 14 is formed in the upper surface of this polycrystalline silicon film 4 so that it may be filled up with a breakthrough. Drawing 4 (c) shows the connecting plug which used the cap insulation film 15 instead of the cap metal membrane 14.

[0100]Drawing 5 is a process sectional view showing other formation methods of the slot 12. This is the formation method which combined RIE or optical etching, and wet etching.

[0101]First, as shown in drawing 5 (a), after the principal surface forms the mask pattern 11 on the silicon substrate 2 of {100}, this mask pattern 11 is used as a mask, the silicon substrate 2 is etched, and sectional shape forms rectangular slot 12_1.

[0102]Here, as etching, RIE or optical etching (photochemistry etching, etching from **** (optical ablation)) is used. Since especially optical etching has an advantage of high-speed etching and a low damage, it is suitable for forming trench 12_1. In photochemistry etching, Cl_2 gas is used as etching gas and ultraviolet rays are used as excitation light, for example.

[0103]Next, as shown in drawing 5 (b), the mask pattern 11 is used as a mask, wet etching of the silicon substrate 2 is carried out, and {111} sides are exposed. As a result, triangular slot 12_2 is formed for sectional shape. As an etching reagent, the KOH solution whose temperature is 60-90 ** is used, for example.

[0104]Next, as shown in the figure (b), the metal balls 16, such as nickel, Ti, Zr, Hf, and V, are arranged in slot 12_2, for example. Specifically, the metal ball 16 is arranged into the portion of the bottom of slot 12_2.

[0105]Next, as shown in drawing 5 (c), by heat treatment, the metal ball 16 and the silicon substrate 2 are made to react, and the metal silicide film 17 is formed in the silicon substrate 2 of the lower part of slot 12_2.

[0106]Next, as shown in drawing 5 (d), etching removal of the metal silicide film 17 is carried out selectively, and trench 12_3 is formed more. Finally, after performing insulator layer formation and metal embedding, a deep breakthrough is obtained by grinding a substrate rear.

[0107]Thus, by making a hole deep gradually, a deep hole can be easily formed now, therefore a deep breakthrough can be easily formed now.

[0108]Other formation methods of a penetration plug are shown in drawing 6.

[0109]After drawing 6 (a) applies the conductive paste 18 as a penetration plug to the whole surface, it makes the conductive paste 18 mobilize by heat treatment, and shows how to embed the conductive paste 18 at Mizouchi. Then, the excessive conductive paste 18 outside a slot is removed using the CMP method etc.

[0110]After drawing 6 (b) deposits two or more metal particles 19 as a penetration plug on the whole surface and embeds Mizouchi by the particles 19, it shows how to remove the excessive metal particles 19 outside a slot using the CMP method etc.

[0111]The solvent (suspension) in which metal grains were distributed may be used instead of the metal particles 19.

[0112]After drawing 6 (c) deposits the silicone film 20 on the whole surface and then deposits high-

melting point metal membranes (un-illustrating), such as a Ti film, on the silicone film 20, it shows how to form the metal silicide film 21 as a penetration plug by heat treatment. Then, the excessive metal silicide film 21 outside a slot is removed using the CMP method etc.

[0113]A silicone film is deposited on an insulator layer conformal one. Therefore, since the silicone film 20 covers Mizouchi's whole velum film 5 even if a slot is deep, it becomes possible to form the metal silicide film 21 which covers the side of a slot, and the whole surface at the bottom. When a cavity part remains in Mizouchi, it is good to bury, for example by a low stress film.

[0114]Another formation method of a penetration plug is shown in drawing 7.

[0115]First, as shown in drawing 7 (a), the side of the slot 12 and the whole surface at the bottom are covered, but the silicone film 22 of the thickness which is not filled up with the inside of the slot 12 is formed. Then, as shown in the figure (a), the nickel grain 23 (metal ball) about 10 micrometers in diameter is arranged in the slot 12.

[0116]Next, as shown in drawing 7 (b), by heat treatment, the silicone film 22 and the nickel grain 23 are made to react, and the nickel silicide film 24 as a penetration plug is formed in the slot 12. Here, since there are no silicone film 22 and nickel grain 23 of quantity sufficient in the slot 12, a cavity part remains in the upper part of the nickel silicide film 24.

[0117]As finally shown in drawing 7 (c), after depositing the insulator layer or metal membrane used as the cap film 25 on the whole surface, this insulator layer or metal membrane is ground, and the cavity part of the upper part of the nickel silicide film 24 is filled up with the cap film 25.

[0118]the method (a CVD method.) which had described the method of forming a penetration plug so far Various methods, such as not the thing limited to a sputtering technique, plating, the method using conductive paste, the method using metal particles, the method using a metal ball, and the method using suspension but a method which combined these methods suitably, are possible.

[0119](A 3rd embodiment) Drawing 8 is a sectional view of the multichip semiconductor device concerning a 3rd embodiment of this invention. Drawing 9 is a top view of the connection substrate of the multichip semiconductor device of drawing 8.

[0120]There is the feature of this multichip semiconductor device in having electrically connected mutually two chips of the adjacent upper and lower sides via the connection substrate which has a penetration plug and a heater.

[0121]That is, it connected with the penetration plug 4 of connection substrate 31_1 via the solder bump 8, and the pad 6 provided in the multilayer interconnection layer 3 of chip 1_1 has connected the penetration plug 4 of this connection substrate 31_1 to the penetration plug 4 of chip 1_2 via the solder bump 8.

[0122]Thus, two chip 1_1 of the adjacent upper and lower sides and 1_2 will electrically be mutually connected via the penetration plug 4 of connection substrate 31_1 provided between them. Similarly, chip 1_2 will electrically be connected with chip 1_3 via the penetration plug 4 of connection substrate 31_2. The formation method of the penetration plug 4 applies to it of a 2nd embodiment correspondingly.

[0123]Connection substrate 31_1 and 31_2 are formed so that thermal conductivity may become high enough rather than chip 1_1 - 1_3.

[0124]Specifically, the component of connection substrate 31_1 and 31_2 is formed of insulating materials, such as the material whose thermal conductivity is higher than the silicon which is a component of the silicon substrate 2, for example, SiC, and SiN. The thing in case the component of connection substrate 31_2 is an insulating material is shown in the figure. For this reason, the insulator layer is not formed in the side of a breakthrough in which the penetration plug 4 was embedded.

[0125]To the inside of a connection substrate main part (penetration plug 4+ connection substrate 31_1, penetration plug 4+ connection substrate 31_2), the metal plate 32 whose thermal conductivity is higher than it is embedded. The components of this metal plate 32 are metal, such as W and Cu, for example. The metal plate 32 may be formed in the surface of connection substrate 31_1 and 31_2, and may be provided in both an inside and the surface.

[0126]The heater 33 embeds and is formed in the surface and the rear face of connection substrate 31_1 and 31_2 so that the solder bump's 8 periphery may be surrounded, respectively. The heater 33 is connected to the external power via the power source line 34 which consists of W etc. which were provided in connection substrate 31_1 and 31_2.

[0127]Each power source line 34 is independently controllable, The heater 33 by which embedding formation was carried out, respectively, i.e., four heaters, can be independently controlled now, respectively at the surface and the rear face of the heater 33 by which embedding formation was carried out by this at the surface and the rear face of connection substrate 31_1, respectively, and connection substrate 31_2. The power source line 34 constitutes a capacitor and supply of the stable power supply is possible for it.

[0128]35 show a wiring board among a figure and 36 shows the multilayer interconnection layer. Although 31_3 shows the same connection substrate as connection substrate 31_1 and 31_2, it is not used for connection of chips. Although this connection substrate 31_3 is used as a heat sink, it is not necessarily required. The insulator layer of the breakthrough side attachment wall of a semiconductor substrate is omitted.

[0129]In this embodiment, connection substrate 31_1 and 31_2 from thermal conductivity being sufficiently higher than chip $1_1 - 1_3$. Even if chip $1_1 - 1_3$ generate heat at the time of operation of chip $1_1 - 1_3$, the heat can be effectively missed outside via connection substrate 31_1 and 31_2. Thereby, degradation of the operating characteristic of chip 1_1 by generation of heat $- 1_3$ and the ephemeralization of chip $1_1 - 1_3$ can be prevented now.

[0130]Only the vamp linked to the chip according to this embodiment provided in connection substrate 31_1 and 31_2, and **** and the independently controllable heater 33 judged that is poor by inspection by what is fused selectively. Since only a poor chip is selectively separable from a connection substrate, a chip can be repaired easily.

[0131]The situation of repair is shown in drawing 10. Although only the reference number required for explanation is given to the figure, the composition of a multichip semiconductor device is the same as what was shown in drawing 8 (also setting to other embodiments the same).

[0132]Drawing 10 (a) shows signs that the chip is inspected with the inspecting probe, and drawing 10 (b) shows signs that chip 1_2 judged that is poor by inspection, and connection substrate 31_2 connected to it are removed. Chip 1_2 and connection substrate 31_1 connected to it may be removed at the process of drawing 10 (b).

[0133]Then, connection substrate 31_2 to chip 1_2 is separated, and a new chip is connected to connection substrate 31_2. Next, connection substrate 31_2 to which this new chip was connected is connected as before. Then, a chip is inspected, if it is success, repair will be ended, but in being a rejection, it repeats the above-mentioned step until it is passing.

[0134]Although the heater 33 was formed so that the solder bump's 8 periphery might be surrounded, and the case where the solder bump's 8 periphery was heated preferentially was explained by this embodiment, even when the heater 33 is formed so that the whole connection substrate may be heated, repair can be easily performed rather than before.

[0135](A 4th embodiment) Drawing 11 is a sectional view of the multichip semiconductor device concerning a 4th embodiment of this invention.
[0136]There is a point that this embodiment differs from a 3rd embodiment in having formed the radiation fin 37 in connection substrate 31_1 - 31_3. This radiation fin 37 is fixed to connection substrate 31_1 - 31_3, for example by adhesives. Other fixing methods, such as fixing, may be used by carrying out metallizing.
[0137]Since it not only misses heat from connection substrate 31_1 - 31_3, but ****** which misses heat also from the radiation fin 37 whose thermal conductivity is higher than it is made according to this embodiment, heat can be more effectively missed from chip 1_1 - 1_3.
[0138](A 5th embodiment) Drawing 12 is a sectional view of the multichip semiconductor device concerning a 5th embodiment of this invention.
[0139]There is a point that this embodiment differs from a 4th embodiment in having formed the radiation fin 37 only in the large chip of calorific value. Here, chip 1_2 and 1_3 suppose that calorific value is larger than chip 1_1. In this case, it becomes unnecessary to provide connection substrate 31_3 as a heat sink in chip 1_3, and minuteness making of a device can be attained about a laminating direction.
[0140](A 6th embodiment) Drawing 13 is a sectional view of the multichip semiconductor device concerning a 6th embodiment of this invention.
[0141]The point that this embodiment differs from a 3rd embodiment multilevel-interconnection-izes the inside of connection substrate 31_2, and there is in having carried out the rearrangement of the wiring. The solder bump 8a connected with the upper left solder bump 8c via the plug 38a, the wiring layer 39a, and the plug 38b, and, specifically, is connecting 8 d of solder bumps to the wiring layer 39b via the plug 38c, without connecting with the solder bump 6c on it, without connecting with the solder bump 8b on it.
[0142]Although the heater 33 is embedded and formed in the surface and the rear face of chip 1_3 and it is provided in the position which is separated from the wiring layers 39a and 39b, the heater 33 may be formed in the inside of chip 1_3, and it may provide in the same layer as the wiring layers 39a and 39b.
[0143](A 7th embodiment) Drawing 14 is a sectional view of the multichip semiconductor device concerning a 7th embodiment of this invention.
[0144]The point that this embodiment differs from a 3rd embodiment forms a capacitor in the inside of a connection substrate, and is shown in having attained stabilization of the power supply supplied to a chip. Explanation of connection substrate 31_3 will form the power source wire 40 and the ground line 41 in connection substrate 31_3 so that the ground line 41 may exist in the upper and lower sides of the power source wire 40. Thereby, two capacitors by which direct continuation was carried out are formed in a sliding direction.
[0145]The component of connection substrate 31_3 is an insulating material. 42 and 43 show wiring among the figure. These pads are omitted although the wiring 42 and 43 is connected to a vamp via a pad, respectively. The same capacitor is formed about other connection substrates (un-illustrating) other than connection substrate 31_3.
[0146](An 8th embodiment) Drawing 15 is a sectional view of the multichip semiconductor device concerning an 8th embodiment of this invention.
[0147]The multichip semiconductor device of this embodiment has composition connected to lower layer Si chip 51_2 and 51_3 by laminated wiring board 52_1 in which the upper Si chip 51_1 was formed by Si, and 52_2. 50 show the element formation side of Si chip 51_1 - 51_3 among the figure.

[0148]The pad 53 provided in Si chip 51 $_1$ is connected to the pad 55 provided in laminated wiring board 52 $_1$ via the solder bump 54. This pad 55 via the wiring layer which was formed in laminated wiring board 52 $_1$ and which is not illustrated, the penetration plug 4 linked to this wiring layer, the pad 56 provided in laminated wiring board 52 $_1$, and the solder bump 57, It has connected with the pad 58 provided in laminated wiring board 52 $_2$. Here, the penetration plug 4 and the above-mentioned wiring layer are good [in order to fully demonstrate the original purpose, metal, such as Cu and aluminum, is usually used, but] to put emphasis on making a coefficient of thermal expansion the same to use what was formed with the Si film of high impurity concentration.
[0149]The pad 58 is connected to the wiring layer which was formed in laminated wiring board 52 $_2$ and which is not illustrated, the pad 59 linked to this wiring layer, and the pad 61 provided in Si chip 51 $_2$ and 51 $_3$ via the solder bump 60. The above-mentioned wiring layer uses a metallic material or the Si film of high impurity concentration, as mentioned above.
[0150]Thus, the upper Si chip 51 $_1$ is connected to lower layer Si chip 51 $_2$ and 51 $_3$ via laminated wiring board 52 $_1$ and 52 $_2$.
[0151]Laminated wiring board 52 $_1$ is connected to laminated wiring board 52 $_2$ via the pad 56, the solder bump 57, and the pad 58. Laminated wiring board 52 $_2$ is similarly connected to the plastic plate 65 via the pad 62, the solder bump 63, and the pad 64. The pad 66 and the solder bump 67 are formed in the plastic plate 65, and the wiring layer 68 which connects between the pads 64 and 66 is formed into the plastic plate 65.
[0152]Between each of Si chip 51 $_2$, and 51 $_3$ and laminated wiring board 52 $_2$, it fills up with the adhesives 69 with which the filler is not mixed between Si chip 51 $_1$ and laminated wiring board 52 $_1$.

[0153]Even if the filler is not mixed in the adhesives 69, the component of Si chip 51 $_1$ - 51 $_3$ and it of laminated wiring board 52 $_1$ and 52 $_2$ are the same Si, Therefore, since the coefficient of thermal expansion of Si chip 51 $_1$ - 51 $_3$ and it of laminated wiring board 52 $_1$ and 52 $_2$ become equal, reliable connection can be obtained.
[0154]Since a component differs between laminated wiring board 52 $_2$ and the plastic plate 65 mutually, on the other hand, between laminated wiring board 52 $_2$ and the plastic plate 65, It fills up with the adhesives 70 with which the filler was mixed, and the reliability of these 52 $_2$ and connection between 65 is secured.
[0155]Here, since the element is not formed in laminated wiring board 52 $_1$ and 52 $_2$, the pitch between the solder bumps 63 can be set as a desired value. Therefore, the pitch between the solder bumps 63 can be taken to such an extent that the adhesives 70 enter certainly between the solder bumps 63.
[0156]Since laminated wiring board 52 $_1$, 52 $_2$ and Si chip 51 $_1$ - 51 $_3$ are formed by the same Si in the embodiment as stated above, heat distortion is hardly produced in the solder bumps 54 and 60.
[0157]Therefore, high integration of Si chip 51 $_1$ - 51 $_3$ progresses further, Even if the distance between the distance between Si chip 51 $_1$ and laminated wiring board 52 $_1$, Si chip 51 $_2$, and 51 $_3$ and laminated wiring board 52 $_2$ becomes short, The reliability of connection between these is secured, therefore can secure now the reliability of connection between the upper Si chip 51 $_1$, and lower layer Si chip 51 $_2$ and 51 $_3$.
[0158]Since laminated wiring board 52 $_1$, 52 $_2$ and Si chip 51 $_1$ - 51 $_3$ are formed by the same Si, the

adhesives 69 in which it is not necessary to bring these coefficients of thermal expansion close to which, therefore the filler is not contained can be used.

[0159]Therefore, high integration of Si chip 51 $_1$ - 51 $_3$ progresses further, Even if the distance between the distance between Si chip 51 $_1$ and laminated wiring board 52 $_1$, Si chip 51 $_2$, and 51 $_3$ and laminated wiring board 52 $_2$ becomes short, Since the portion with which the adhesives 69 are not filled up is not produced, the reliability of connection between the upper Si chip 51 $_1$, and lower layer Si chip 51 $_2$ and 51 $_3$ can be secured.

[0160]Flat-surface area of a device can be made small for the same reason as a 1st embodiment.

[0161]In this embodiment, since it is not necessary to form a penetration plug in Si chip 51 $_1$ in which the element was formed - 51 $_3$, the rise of cost can be controlled. Of course, Si chip 51 $_1$, and Si chip 51 $_2$ and 51 $_3$ may be made the composition connected only via laminated wiring board 52 $_1$ using Si chip 51 $_1$ which has a penetration plug - 51 $_3$.

[0162]Drawing 16 - drawing 18 are the process sectional views showing the manufacturing method of the multichip semiconductor device of this embodiment.

[0163]First, as shown in drawing 16 (a), Si chip 51 $_1$ is created, accumulation formation of the element which is not illustrated to the element formation side 50 of a Si substrate is carried out, then the pad 53 is formed, and the solder bump 54 is continuously formed on the pad 53.

[0164]Next, as shown in drawing 16 (b), the penetration plug 4 and wiring layer which become a Si substrate from Si, and the pad 55 are formed, and laminated wiring board 52 $_1$ is created. The pad 55 is formed in the position corresponding to the pad 33. The pads 33 and 55 are the squares whose one side is 20 micrometers, and the pitch of the pads 33 and 55 is 30 micrometers (the distance between pads is 10 micrometers).

[0165]Next, as shown in drawing 16 (c), alignment of the solder bump 54 of Si chip 51 $_1$ and the pad 55 of laminated wiring board 52 $_1$ is performed, By being filled up with the adhesives 69 of an epoxy system with which the filler is not mixed between Si chip 51 $_1$ and laminated wiring board 52 $_1$ after joining these [54 and 55], Si chip 51 $_1$ forms unit 71 $_1$ which comes to carry out flip chip bonding on laminated wiring board 52 $_1$.

[0166]The distance of the Si substrate which constitutes laminated wiring board 52 $_1$, and the Si substrate which constitutes Si chip 51 $_1$ shall be 20 micrometers. For that purpose, a 20 micrometerphi grade may be sufficient as the size of the solder bump 54.

[0167]Next, as shown in drawing 17 (d), Si chip 51 $_2$ is created, accumulation formation of the element which is not illustrated to the element formation side 50 of a Si substrate is carried out, then the pad 61 is formed, and the solder bump 60 is continuously formed on the pad 61 of Si chip 51 $_2$. Next, as shown in the figure (d), Si chip 51 $_2$ is created similarly, and the solder bump 60 is continuously formed on the pad 61 of Si chip 51 $_2$.

[0168]Next, as shown in drawing 17 (e), the penetration plug 4 and wiring layer, and the pads 58, 59, and 62 which become a Si substrate from Si are formed, laminated wiring board 52 $_2$ is created and then the solder bump 57 is formed on the pad 58.

[0169]Next, as shown in drawing 17 (f), like the case of unit 71 $_1$, Alignment, junction, and restoration of the adhesives 69 are performed and Si chip 51 $_2$ and unit 71 $_2$ to which it comes to carry out flip chip bonding of the 51 $_3$ are formed on laminated wiring board 52 $_2$.

[0170]Next, as shown in drawing 18 (g), unit 71 $_1$ and unit 71 $_2$ are connected by joining the solder

bump 58 and the pad 56.

[0171]Since laminated wiring board 52_1, 52_2, Si chip 51_2 - 51_3 are formed by Si at this time, there is no heat distortion by the difference in a coefficient of thermal expansion. Therefore, the heat distortion by the difference in a coefficient of thermal expansion should just perform the size of each vamp, and the design of a pitch only in consideration of the thickness of laminated wiring board 52_1, Si chip 51_2 between 52_2, and 51_3, without taking into consideration.

[0172]Since it is connected with the solder bump 63 of the plastic plate 65, the pad 62 formed in the undersurface of laminated wiring board 52_2 needs to take 100 micrometers of the diameters and pitches of the pad 62, respectively. [not less than about 200 micrometers of] The wiring layer for easing a pitch is formed in laminated wiring board 52_2.

[0173]Finally, as shown in drawing 18 (h), form the plastic plate 65 which has the pads 64 and 66 and the wiring layer 68, then, form the solder bumps 63 and 67 on the pad 64 and 66, and then the plastic plate 65, After carrying out alignment of the unit 71_2 to which unit 71_1 was connected and joining, In order to ease distortion between the plastic plate 65 and unit 71_2, it is filled up with the adhesives 70 containing the filler of SiO_2, and the multichip semiconductor device shown in drawing 15 is completed.

[0174]According to this embodiment, the Si substrate is used as a substrate of laminated wiring board 52_1 and 52_2. Therefore, cheap and homogeneous laminated wiring board 52_1 and 52_2 can be formed with mass production.

[0175]The design rule of the wiring layer formed in laminated wiring board 52_1 and 52_2 is far loose compared with it of the wiring layer formed in Si chip 51_1 and 51_2 (for example, several micrometers order). Therefore, the yield can also obtain about 100%. Since it is not necessary to form elements, such as a MOS transistor and a capacitor, there is almost no necessity of taking contamination of a Si substrate into consideration, and a process can also be simplified.

[0176]Although this embodiment explained the case where the component of a laminated wiring board was the same as the component of a chip, as long as a coefficient of thermal expansion is almost equal, components may differ. The combination of the component to which the heat dissipation nature of a laminated wiring board (connection substrate) becomes high is better than a chip so that he may like to explain by the paragraph of an operation in this case.

[0177]In the case of the same component, it is good to form a penetration plug, for example with the material whose heat dissipation nature is higher than the component of a laminated wiring board by providing the radiation means of a radiation fin etc. in a laminated wiring board, or giving a radiating function to it at the penetration plug formed in a laminated wiring board. If it is a case where the component of a chip and a laminated wiring board is Si, specifically, it turns out that what is necessary is just to use SiC and AlN from Table 1.

[0178]

[Effect of the Invention]Since two or more chips are laminated according to the 1st this invention as explained in full detail above, Flat-surface area of a device can be made small, and since it becomes possible to apply an inspecting probe to the above-mentioned conductive plug easily by arranging the chip with which the conductive plug was moreover formed at the top or the bottom, a device can be inspected easily.

[0179]Since two or more chips are laminated according to the 2nd this invention, flat-surface area of a device can be made small, and moreover, since heat dissipation nature is higher than a chip, the way of a connection substrate can aim at the improvement of heat dissipation nature.

[0180]Since two or more chips are laminated according to the 3rd this invention, flat-surface area of a device can be made small, moreover, by the exothermic part of a connection substrate, the vamp linked to a poor chip can be fused and, thereby, a chip can be repaired easily.

[0181]Since two or more chips are laminated according to the 4th invention, can make flat-surface area of a device small, and moreover, since the coefficient of thermal expansion of the component of a connection substrate and it of the component of a semiconductor substrate are almost equal, Even if it uses a vamp and adhesives for a connecting member, the reliability of connection during an up-and-down chip can be secured.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention]This invention relates to the multichip semiconductor device which is a semiconductor device which used two or more chips.

[Translation done.]

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PRIOR ART

[Description of the Prior Art]In recent years, many transistors, resistance, etc. are connected to the significant part of a computer or communication equipment so that an electric circuit may be attained, and the large scale integration circuit (chip) integrated and formed on the semiconductor substrate is used abundantly. For this reason, the performance of the whole apparatus is connected as greatly as the performance of a chip simple substance.
[0003]On the other hand, what is called a multichip semiconductor device that planned the performance of the whole apparatus is also proposed using two or more chips. The sectional view of the conventional multichip semiconductor device is shown in drawing 19 - drawing 24.
[0004]Drawing 19 shows the multichip semiconductor device of the type which carries out plane configuration of two or more chips 82 on the wiring board 81 of lamination, for example. 83 show the solder bump among the figure.
[0005]Drawing 20 shows the multichip semiconductor device of the type which makes the surface facing each other (Face to Face), and connects chips.
[0006]Drawing 21 shows the multichip semiconductor device of the type which carries out lamination arrangement of two or more chips 82 using the laminate sheet 84.
[0007]Drawing 22 shows the multichip semiconductor device which used wire bonding as a mounting method.
The pad (un-illustrating) of the Si chip 91 is connected with the leadframe 94 of the laminate sheet 93 by the bonding wire 92.

[0008]Drawing 23 shows the multichip semiconductor device which used TAB (Tape Automated Bonding) as a mounting method.
The pad of the Si chip 91 is connected to the pad (un-illustrating) of the laminate sheet 93 via the solder bump 95 and TAB lead 96.

[0009]In drawing 22 and drawing 23, 97 shows a socket and 98 shows the connector pin.
[0010]Drawing 24 shows the multichip semiconductor device which used the flip chip as a mounting method.
The pad 100 arranged in the shape of a lattice all over the Si chip 91 is connected with the pad 101 similarly arranged in the shape of a lattice all over the laminate sheet 99 via the solder bump 102.

[0011]In drawing 24, 103 shows the adhesives of the epoxy resin system containing a filler, it fills up with these adhesives 103 between the Si chip 91 and the laminate sheet 99, and they carry out adhesion immobilization of these [91 and 93]. 104,105,107 shows a pad and 106,108 shows the solder bump.

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EFFECT OF THE INVENTION

[Effect of the Invention]As explained in full detail above, two or more chips are laminated in the 1st this invention.
Therefore, flat-surface area of a device can be made small, and since it becomes possible to apply an inspecting probe to the above-mentioned conductive plug easily by arranging the chip with which the conductive plug was moreover formed at the top or the bottom, a device can be inspected easily.

[0179]Two or more chips are laminated in the 2nd this invention.
Therefore, flat-surface area of a device can be made small, and moreover, since heat dissipation nature is higher than a chip, the way of a connection substrate can aim at the improvement of heat dissipation nature.

[0180]Two or more chips are laminated in the 3rd this invention.
Therefore, flat-surface area of a device can be made small, moreover, by the exothermic part of a connection substrate, the vamp linked to a poor chip can be fused and, thereby, a chip can be easily repaired now.

[0181]Two or more chips are laminated in the 4th invention.
Therefore, since the coefficient of thermal expansion of the component of a connection substrate and it of the component of a semiconductor substrate are moreover almost equal, even if it can make flat-surface area of a device small, and it uses a vamp and adhesives for a connecting member, the reliability of connection during an up-and-down chip can be secured.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, there are the following problems in these conventional multichip semiconductor devices.
[0013]That is, in order that the conventional multichip semiconductor device of drawing 19 may carry out plane configuration of two or more chips 82, there is a problem that the flat-surface area of a device is large.
[0014]In order that the conventional multichip semiconductor device of drawing 20 may laminate two or more chips 82, there is no problem that the flat-surface area of a device becomes large, but there is a problem that lamination number of sheets is limited to two sheets. The problem of being difficult also has the inspection of a device.
[0015]Since the conventional multichip semiconductor device of drawing 21 can laminate two or more chips 82, Although neither the problem which becomes large, nor the problem that lamination number of sheets is limited to two sheets has the flat-surface area of a device, melting of the vamp 83 on the specific chip 82 cannot be carried out selectively, and there is a problem that repair of the chip 82 is difficult. Although a chip generates heat at the time of operation of a chip, since the heat cannot be missed outside effectively, there is a problem that the operating characteristic of a chip deteriorates or the life of a chip becomes short.
[0016]The conventional multichip semiconductor device of drawing 22 a pad with a narrow pitch of the Si chip 91 integrated highly by the bonding wire 92. In order to connect with the leadframe 94 of the laminate sheet 93, it is necessary to carry out alignment of between forming wiring on the laminate sheet 93, and a chip and a laminate sheet in high accuracy, and connection is becoming difficult.
[0017]In order that the conventional multichip semiconductor device of drawing 22 and drawing 23 may connect laminate sheet 93 comrades using the socket 97 and the connector pin 98, a certain amount of height is needed, and there is a problem that the connection gap at the time of laminating is large, and integration of a lengthwise direction is difficult.
[0018]Although this kind of problem is solvable by using the conventional multichip semiconductor device of drawing 24, there are the following problems in the multichip semiconductor device of drawing 24.
[0019]Since the shape of the solder bump 102 is a hard drum form, when high integration of the Si chip 91 progresses further and the size and the pitch interval of the pad 100,101 contract further, If distance (connecting distances) between the Si chip 91 and the laminate sheet 99 is shortened and the path of the solder bump 102 is not made small, the faulty connection that the solder bump 102 of next doors short-circuits will arise.
[0020]However, since the laminate sheet 99 is formed to the Si chip 91 being formed using a Si substrate using the plastic plate which consists of glass epoxy etc., A coefficient of thermal expansion differs between the Si chip 91 and the laminate sheet 99 mutually, if connecting distances are shortened as the result, heat distortion will arise in the solder bump 102, and fatigue breaking

will produce them by the repetition which is a thermal excursion. Heat distortion is so large that connecting distances are short, and a fatigue life becomes short. Therefore, the reliability of connection between the Si chip 91 and the laminate sheet 99 falls, so that connecting distances are short.

[0021]SiO_2 which there is a role which makes such heat distortion small in the adhesives 103 with which it filled up between the Si chip 91 and the laminate sheet 99, therefore can bring both coefficient of thermal expansion close is mixed as a filler.

[0022]Although the size of a filler is about 10-30 micrometers, Since the portion with which the adhesives 103 are not filled up will arise if connecting distances become short, the problem of it becoming impossible to secure the reliability of connection between the Si chip 91 and the laminate sheet 99, but to also secure the reliability of connection during the up-and-down Si chip 91 as the result arises.

[0023]It is in providing the multichip semiconductor device this invention was made in consideration of the above-mentioned situation, and it becomes the place made into the purpose (the 1st purpose) has a small flat-surface area of a device, and possible to inspect a device easily.

[0024]Other purposes (the 2nd purpose) of this invention have a small flat-surface area of a device, and there is in providing the multichip semiconductor device excellent in heat dissipation nature.

[0025]Other purposes (the 3rd purpose) of this invention have a small flat-surface area of a device, and there is in providing the multichip semiconductor device which can repair easily.

[0026]Other purposes (the 4th purpose) of this invention have a small flat-surface area of a device, and there is in providing the multichip semiconductor device which can secure the reliability of connection during an up-and-down chip.

[Translation done.]

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MEANS

[Means for Solving the Problem][Elements of the Invention] -- a multichip semiconductor device (claim 1) concerning this invention, in order to attain the 1st purpose of an account of a top, In a multichip semiconductor device with which an element carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, Two chips of the adjacent upper and lower sides electrically connected mutually via a connection substrate provided among these, and a conductive plug which a breakthrough was formed in said semiconductor substrate and formed in this breakthrough has connected with said connection substrate.
[0028]Here, a breakthrough may be provided in both two both [one side or] of a semiconductor substrate.
[0029]A multichip semiconductor device (claim 2) applied to this invention in order to attain the 2nd purpose of the above, In a multichip semiconductor device with which an element carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate by which ** was formed between two chips of the adjacent upper and lower sides, and a conductive plug was formed in a breakthrough is provided, said two chips electrically connect mutually via said conductive plug, and said connection substrate is characterized by heat dissipation nature being higher than said chip.
[0030]In the above-mentioned multichip semiconductor device (claims 1 and 2), as for other multichip semiconductor devices (claim 3) concerning this invention, a substance in which heat dissipation nature becomes high rather than said chip in said connection substrate is chosen as a component of said connection substrate.
[0031]If it is a case of Si chip, specifically, insulating materials, such as SiC and SiN, will be used for a component of a connection substrate.
[0032]Other multichip semiconductor devices (claim 4) concerning this invention, In the above-mentioned multichip semiconductor device (claims 1 and 2), said connection substrate comprises a connection substrate main part in which said conductive plug was formed, and a high temperature conductivity member whose thermal conductivity is higher than this connection substrate main part.

[0033]If a component of a connection substrate is a case of insulating materials, such as SiC, specifically, a member which comprised metallic materials, such as W and Cu, will be used for a high temperature conductivity member.
[0034]Other multichip semiconductor devices (claim 5) concerning this invention are characterized by said high temperature conductivity members being the conductive plates formed in an inside of said connection substrate main part in the above-mentioned multichip semiconductor device (claim 4).
[0035]Here, conductive plates may be provided on the surface of a connection substrate. Conductive plates may be provided in both an inside of a connection substrate, and the surface.

[0036]Other multichip semiconductor devices (claim 6) concerning this invention are characterized by said high temperature conductivity member being the radiation fin provided in the surface of said connection substrate main part in the above-mentioned multichip semiconductor device (claim 4).
[0037]Here, a radiation fin may be provided in all the connection substrates, or it may provide in a specific connection substrate, for example, a low connection substrate of heat dissipation nature.
[0038]A multichip semiconductor device (claim 7) applied to this invention in order to attain the 3rd purpose of the above, In a multichip semiconductor device with which an element carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate by which ** was formed between two chips of the adjacent upper and lower sides, and a conductive plug was formed in a breakthrough is provided, said two chips electrically connect with said conductive plug via a vamp, respectively, and, as for said connection substrate, it has an exothermic part.
[0039]Other multichip semiconductor devices (claim 8) concerning this invention can control an exothermic part of each connection substrate independently in the above-mentioned multichip semiconductor device (claim 7).
[0040]A multichip semiconductor device (claim 12) applied to this invention in order to attain the 4th purpose of the above, Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate in which it comes to form a conductive plug is provided in a breakthrough, and said two chips are electrically mutually connected via said conductive plug, And as for said connection substrate, a component of said connection substrate has the almost same coefficient of thermal expansion as it of said semiconductor substrate more highly [heat dissipation nature] than said chip.
[0041]Other multichip semiconductor devices (claim 13) applied to this invention in order to attain the 4th purpose of the above, Between two up-and-down chips with which an element adjoins each other in a multichip semiconductor device which carries out the plural laminates of the chip which has the semiconductor substrate by which accumulation formation was carried out, A connection substrate which it comes to form a conductive plug in a breakthrough is provided, and via said conductive plug, it electrically connects mutually and, as for a component of said connection substrate, said two chips have the almost same coefficient of thermal expansion as it of said semiconductor substrate.

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OPERATION

[OPERATION] Since two or more chips are laminated according to the 1st this invention (claim 1), unlike the conventional multichip semiconductor device which carries out the plane position of two or more chips, flat-surface area of a device can be made small.
[0043]Since it will become possible to apply an inspecting probe to the above-mentioned conductive plug easily if the chip with which the conductive plug was formed according to the 1st this invention is arranged at the top or the bottom, a device can be inspected easily.
[0044]According to the 2nd this invention (claims 2-6), flat-surface area of a device can be made small for the same reason as the 1st this invention (claim 1).
[0045]In the 2nd this invention, the connection substrate of heat dissipation nature is higher than a chip.
Therefore, the heat of a chip can be effectively missed outside via a connection substrate.
And degradation of the operating characteristic of a chip and the ephemeralization of a chip by a chip generating heat at the time of operation of a chip can be prevented now by improving heat dissipation nature in this way.
[0046]According to the 3rd this invention (claims 7-9), flat-surface area of a device can be made small for the same reason as the 1st this invention (claim 1).
[0047]In the 3rd this invention, a poor chip is separable from a connection substrate by fusing the vamp linked to a poor chip by the exothermic part of a connection substrate.
Therefore, a chip can be easily repaired now.
Especially in the case of this invention (claim 8), since the exothermic part of each connection substrate is independently controllable, a chip can be repaired more easily.
[0048]According to the 4th this invention (claims 12-14), flat-surface area of a device can be made small for the same reason as the 1st this invention (claim 1).
[0049]In the 4th this invention, it of the coefficient of thermal expansion of the component of a connection substrate and the component of a semiconductor substrate is almost equal.
Therefore, in order to connect a connection substrate and a semiconductor substrate, even if it uses a vamp, heat distortion is hardly produced by a vamp.

[0050]Therefore, even if high integration of a chip progresses further and the distance between a chip and a connection substrate becomes short, the reliability of connection between a connection substrate and a semiconductor substrate can be secured, therefore the reliability of connection during an up-and-down chip can be secured.
[0051]Since it of the coefficient of thermal expansion of the component of a connection substrate and the component of a semiconductor substrate is almost equal, in order to bring both coefficient of thermal expansion close, it is not necessary to use the adhesives containing a filler.
[0052]Therefore, even if high integration of a chip progresses further and the distance between a connection substrate and a semiconductor substrate becomes short, it does not produce, but the

reliability of connection between a chip and a connection substrate is in the portion with which adhesives are not filled up by reservation, therefore it can secure the reliability of connection during an up-and-down chip.

[0053]The thermal conductivity and coefficient of linear expansion of the main substances used for the component of a semiconductor substrate and the component of a connection substrate which are used for a chip are shown in Table 1.

[0054]

[Table 1]

材　料	熱伝導率λ ($Wm^{-1}K^{-1}$)	線膨張率α (10^{-6})
シリコン(Si)	150	2.5
ガリウム砒素(GaAs)	50	5.8
二酸化シリコン(SiO_2)	1	0.5
窒化シリコン(Si_3N_4)	2.3	1.5
ベリリア(BeO)	200	6.0
アルミナ(Al_2O_3)	30	6.0
シリコンカーバイド(SiC)	220	3.7
窒化アルミニウム(AlN)	230	4.3
ポリイミド	0.4	45.0
エポキシガラス(プリント基板)	0.3	15.0

[0055]If the component of the connection substrate in this invention is a case where the component of a semiconductor substrate is Si, for example, in respect of relaxation of heat distortion, its Si of the material is the best, but the silicon carbide (SiC) whose Si and coefficient of linear expansion are almost equal, and alumimium nitride (AlN) may be sufficient as it. Since thermal conductivity is higher than Si, these are excellent also in respect of heat dissipation nature.

[0056]When the component of the semiconductor substrate used for a chip is a compound semiconductor, in being gallium arsenide (GaAs), for example, GaAs, beryllia (BeO), and alumina (aluminum$_2O_3$) are suitable.

[0057]Although it is dependent on the size of a contact button (pad), and a pitch and the size of a connection substrate, how many differences of thermal expansion can approve, As for the difference of the coefficient of thermal expansion of the component of a connection substrate, and that of the component of a semiconductor substrate, for reservation of the reliability of connection during the chip made into the purpose of this invention, it is preferred that it is less than **5.0x10 $^{-6}$.

[0058]

[Embodiment of the Invention]Hereafter, an embodiment of the invention (henceforth an embodiment) is described, referring to drawings.

[0059](A 1st embodiment) Drawing 1 is a sectional view of the multichip semiconductor device concerning a 1st embodiment of this invention.

[0060]This multichip semiconductor device has the composition that two chip 1 $_1$ and 1 $_2$ were connected via the laminated wiring board 9 made from ceramics. Chip 1 $_1$ and 1 $_2$ are roughly divided, and comprise the silicon substrate 2 by which accumulation formation of the element was carried out, and the multilayer interconnection layer 3 for connecting an element to a predetermined relation.

[0061]The pad 6 provided in the multilayer interconnection layer 3 of chip $_1$ is electrically connected to the pad 6 provided in the laminated wiring board 9 via the solder bump 8. Other pads 6 provided

in the laminated wiring board 9 electrically connected to this pad 6 are electrically connected to the pad 6 provided in the multilayer interconnection layer 3 of chip 1_2. Thus, two up-and-down chip 1_1 and chip 1_2 will electrically be mutually connected via the laminated wiring board 9 formed among these.

[0062]The conductive penetration plug 4 (conductive plug) which penetrates the silicon substrate 2 is formed in chip 1_2. This penetration plug 4 is electrically connected to the pad 6 provided in chip 1_2, and the pad 6 provided in the laminated wiring board 9 via the vamp 8 on it.

[0063]The penetration plug 4 is formed in the outside of an element formation region, and the insulator layer 5 is formed between the penetration plug 4 and the silicon substrate 2 (breakthrough). The connecting plug comprises this insulator layer 5 and the penetration plug 4.

[0064]The silicon field of the silicon substrate 2 of an opposite hand, i.e., fields other than penetration plug 4, is covered with the insulator layer 7 in the multilayer interconnection layer 3 of chip 1_2. There is an effect which promotes heat dissipation in such a penetration plug 4.

[0065]As other means to promote heat dissipation, forming the laminated wiring board 9 with the material whose thermal conductivity is higher than chip 1_1 and 1_2 is raised. If it is a case of Si chip, specifically, insulating materials, such as SiC and SiN, will be raised. A metal plate may also be embedded inside so that a 2nd embodiment may explain.

[0066]Since chip 1_2 is laminated via the laminated wiring board 9 on chip 1_1 according to this embodiment, unlike the conventional multichip semiconductor device which carries out the plane position of two or more chips, flat-surface area of a device can be made small.

[0067]Since chip 1_2 which has the penetration plug 4 which electrically connected with chip 1_1 via the laminated wiring board 9 is used according to this embodiment, a device can be inspected by applying an inspecting probe to the penetration plug 4. Here, since it has exposed to the rear face of the semiconductor substrate 2, the penetration plug 4 can hit an inspecting probe to the penetration plug 4 easily. Therefore, according to this embodiment, it is so that a device can be inspected easily.

[0068]Although the case where a chip was two pieces was explained here, At this embodiment, since chips are connected with the laminated wiring board 9, unlike the conventional multichip semiconductor device which connects chips by Face to Face, there is no problem that the lamination number of sheets of a chip is limited to two sheets.

[0069]Therefore, according to this embodiment, the multichip semiconductor device which the flat-surface area of a device is small, and can inspect a device easily and with which lamination number of sheets is not limited to two sheets can be realized now.

[0070]In this embodiment, although the penetration plug 4 was formed in chip 1_2, it may provide in chip 1_1, or may provide in both chip 1_1 and 1_2.

[0071](A 2nd embodiment) Drawing 2 and drawing 3 are the process sectional views showing the formation method of the penetration plug 4 of the multichip semiconductor device of drawing 1. In the following figures, the above-mentioned figure and identical codes show identical parts or a considerable portion, and detailed explanation is omitted.

[0072]First, as shown in drawing 2 (a), the silicon substrate 2 is prepared. The thing of which stage after the element formation in the middle of element formation may be sufficient as this silicon substrate 2 before isolation and after isolation.

[0073]The substrate after forming before element formation and the STI isolation back in the field enclosed with a round mark among the figure and forming a protective film (BPSG) on a MOS transistor (after element formation) is shown. As after element formation, it is raised, after forming wiring in others.

[0074]As the element formation middle, the next process after forming a required well in a substrate

face by an ion implantation, and the next process after forming a gate electrode are raised, for example.

[0075]Next, as shown in drawing 2 (b), after forming the mask pattern 11 with a thickness of 1 micrometer which consists of SiO_2 on the silicon substrate 2, Etching gas etches the silicon substrate 2 selectively by using the mask pattern 11 as a mask using RIE of gas F system, and forms the 100-micrometer-deep slot 12 in the surface of the silicon substrate 2. This slot 12 serves as a breakthrough eventually.

[0076]Here, although the component used the mask pattern 11 of SiO_2 instead, a component may use the mask pattern 11 of the material which has a high selection ratio to Si, such as aluminum and aluminum$_2O_3$.

[0077]The processing technology which forms the slot 12 (breakthrough) is not limited to RIE, and can also use optical etching, wet etching, ultrasonic machining, and an electron discharge method. The above-mentioned processing technology may be combined suitably. The method which combined RIE or optical etching, and wet etching is explained later.

[0078]Next, as shown in drawing 2 (c), after removing the mask pattern 11, use an LPCVD method for the whole surface and a 100-nm-thick SiO_2 film and a 100-nm-thick Si_3N_4 film are deposited on it one by one, The insulator layer 5 of the laminated structure which consists of a SiO_2 film and an Si_3N_4 film is formed. The insulator layer of a monolayer may be used instead of the insulator layer 5 of a laminated structure.

[0079]Next, as shown in drawing 2 (d), the polycrystalline silicon film 4 of low resistance used as a penetration plug in which impurities, such as B, were doped is formed in the whole surface at thickness overflowing from the slot 12, and the inside of the slot 12 is embedded with the polycrystalline silicon film 4.

[0080]As a formation method of the polycrystalline silicon film 4, a CVD method and a sputtering technique are used, for example. Plating can also be used when using a metal membrane instead of the polycrystalline silicon film 4.

[0081]Here, although the polycrystalline silicon film 4 in which the impurity was doped was used as a conductive film used as a penetration plug instead, the amorphous silicon film in which the impurity was doped may be used. Metal, such as W film, a Mo film, a Ni film, and a Ti film, or these metal silicide films may be used.

[0082]Next, the polycrystalline silicon film 4 and the insulator layer 5 are retreated until the surface of the silicon substrate 2 is exposed using methods, such as the CMP method and the etchback method, as shown in drawing 3 (a). As a result, the structure where the polycrystalline silicon film (penetration plug) 4 was embedded via the insulator layer 5 in the slot 12 is formed.

[0083]Next, as shown in drawing 3 (b), the multilayer interconnection layer 3 is formed on the silicon substrate 2 of the side in which the penetration plug 4 was formed. Before forming this multilayer interconnection layer 3, isolation and element formation are performed. Subsequently, the pad 6 is formed in this slot after forming a slot in the surface of this multilayer interconnection layer 3.

[0084]Next, the silicon substrate 2 is retreated until the insulator layer 5 of the pars basilaris ossis occipitalis of the slot 12 exposes the surface (henceforth a rear face) of the silicon substrate 2 of the side and opposite hand in which the penetration plug 4 was formed, as shown in drawing 3 (c). Retreat (thinning) of the silicon substrate 2 is performed by the method which used the processing technology of CMP, chemical polishing, mechanical polishing, wet etching, plasma etching, or vapor etching, or the method which combined these processing technology, for example.

[0085]Next, the rear face of the silicon substrate 2 is selectively etched until the insulator layer 5 of the side attachment wall of the slot 12 above the insulator layer 5 of the pars basilaris ossis occipitalis of the slot 12 is exposed, as shown in drawing 3 (d). CDE, RIE, or wet etching is used for this etching, for example.

[0086]Next, as shown in the figure (d), the insulator layer 7 (the 2nd insulator layer) which consists of SiO_2 is deposited on the rear face of the silicon substrate 2 using plasma CVD method.

[0087]When a low temperature process is required, it is good to use coating films, such as a SOG film, instead of the insulator layer 7 which consists of SiO_2. It is good to make small the stress which the silicon substrate 2 receives to use the insulator layer which consists of organic materials, such as polyimide, instead of SiO_2.

[0088]Next, the penetration plug 4 and the insulator layers 5 and 7 are ground using the CMP method until the rear face of the silicon substrate 2 is exposed, as shown in drawing 3 (e).

[0089]As a result, the structure where the penetration plug (polycrystalline silicon film 4) was embedded at the breakthrough (slot 12), and the silicon field of the rear face of the silicon substrate 2 was covered with the insulator layer 7 is formed.

[0090]As stated above, after forming in the surface of the silicon substrate 2 the slot 12 which does not penetrate this silicon substrate 2, by this embodiment, the structure where the breakthrough (slot 12) was embedded with the penetration plug (polycrystalline silicon film 4) is formed by grinding silicon substrate 2 grade from a rear face.

[0091]Therefore, since according to this embodiment it is not necessary to form a deep breakthrough even if the silicon substrate 2 of a basis is thick (usually thick), the structure where the breakthrough (slot 12) was embedded by the connecting plug (the polycrystalline silicon film 4, the insulator layer 5) can be formed easily.

[0092]With the insulator layer 7, when there is no wrap necessity, a silicon field on the back, At the process of drawing 3 (c), the structure where the breakthrough (slot 12) was embedded by the connecting plug (the polycrystalline silicon film 4, the insulator layer 5) is completed by grinding the silicon substrate 2 and the insulator layer 5 until the polycrystalline silicon film 4 is exposed.

[0093]As for polish (retreat) of the silicon substrate 2, it is preferred to carry out, after starting the silicon substrate 2 from a wafer. It is because a wafer is generally large, and a mechanical strength is weak, so it is difficult to grind uniformly (retreat).

[0094]The sectional view of the connecting plug of various structures is shown in drawing 4. This is a sectional view equivalent to the process of drawing 3 (b). In the figure, the multilayer interconnection layer 3, the pad 6, and the insulator layer 7 are omitted.

[0095]Drawing 4 (a) shows the connecting plug which has the low stress film 13.

[0096]That is, the outside of this connecting plug comprises the conductive film 4a, and the inside comprises the low stress film 13 in which the difference of a coefficient of thermal expansion with the semiconductor substrate 2a is smaller than the conductive film 4a.

[0097]Any of an insulator layer, semiconductor membrane, and a metal membrane may be sufficient as the low stress film 13. The stress which the silicon substrate 2 receives can be reduced now by using such a connecting plug.

[0098]Like this embodiment, when the component (silicon) of a penetration plug (polycrystalline silicon film 4) and a semiconductor substrate (silicon substrate 2) is the same, such a structure is not necessarily required.

[0099]Drawing 4 (b) shows the connecting plug which has the cap metal membrane 14. That is, the polycrystalline silicon film 4 is not formed only by Mr. Fukashi in the middle of a breakthrough, but the cap metal membrane 14 is formed in the upper surface of this polycrystalline silicon film 4 so that it may be filled up with a breakthrough. Drawing 4 (c) shows the connecting plug which used the cap insulation film 15 instead of the cap metal membrane 14.

[0100]Drawing 5 is a process sectional view showing other formation methods of the slot 12. This is the formation method which combined RIE or optical etching, and wet etching.

[0101]First, as shown in drawing 5 (a), after the principal surface forms the mask pattern 11 on the silicon substrate 2 of {100}, this mask pattern 11 is used as a mask, the silicon substrate 2 is etched, and sectional shape forms rectangular slot 12_1.

[0102]Here, as etching, RIE or optical etching (photochemistry etching, etching from **** (optical ablation)) is used. Since especially optical etching has an advantage of high-speed etching and a low damage, it is suitable for forming trench 12_1. In photochemistry etching, Cl_2 gas is used as etching gas and ultraviolet rays are used as excitation light, for example.
[0103]Next, as shown in drawing 5 (b), the mask pattern 11 is used as a mask, wet etching of the silicon substrate 2 is carried out, and {111} sides are exposed. As a result, triangular slot 12_2 is formed for sectional shape. As an etching reagent, the KOH solution whose temperature is 60-90 ** is used, for example.
[0104]Next, as shown in the figure (b), the metal balls 16, such as nickel, Ti, Zr, Hf, and V, are arranged in slot 12_2, for example. Specifically, the metal ball 16 is arranged into the portion of the bottom of slot 12_2.
[0105]Next, as shown in drawing 5 (c), by heat treatment, the metal ball 16 and the silicon substrate 2 are made to react, and the metal silicide film 17 is formed in the silicon substrate 2 of the lower part of slot 12_2.
[0106]Next, as shown in drawing 5 (d), etching removal of the metal silicide film 17 is carried out selectively, and trench 12_3 is formed more. Finally, after performing insulator layer formation and metal embedding, a deep breakthrough is obtained by grinding a substrate rear.
[0107]Thus, by making a hole deep gradually, a deep hole can be easily formed now, therefore a deep breakthrough can be easily formed now.
[0108]Other formation methods of a penetration plug are shown in drawing 6.
[0109]After drawing 6 (a) applies the conductive paste 18 as a penetration plug to the whole surface, it makes the conductive paste 18 mobilize by heat treatment, and shows how to embed the conductive paste 18 at Mizouchi. Then, the excessive conductive paste 18 outside a slot is removed using the CMP method etc.
[0110]After drawing 6 (b) deposits two or more metal particles 19 as a penetration plug on the whole surface and embeds Mizouchi by the particles 19, it shows how to remove the excessive metal particles 19 outside a slot using the CMP method etc.
[0111]The solvent (suspension) in which metal grains were distributed may be used instead of the metal particles 19.
[0112]After drawing 6 (c) deposits the silicone film 20 on the whole surface and then deposits high-melting point metal membranes (un-illustrating), such as a Ti film, on the silicone film 20, it shows how to form the metal silicide film 21 as a penetration plug by heat treatment. Then, the excessive metal silicide film 21 outside a slot is removed using the CMP method etc.
[0113]A silicone film is deposited on an insulator layer conformal one. Therefore, since the silicone film 20 covers Mizouchi's whole velum film 5 even if a slot is deep, it becomes possible to form the metal silicide film 21 which covers the side of a slot, and the whole surface at the bottom. When a cavity part remains in Mizouchi, it is good to bury, for example by a low stress film.
[0114]Another formation method of a penetration plug is shown in drawing 7.
[0115]First, as shown in drawing 7 (a), the side of the slot 12 and the whole surface at the bottom are covered, but the silicone film 22 of the thickness which is not filled up with the inside of the slot 12 is formed. Then, as shown in the figure (a), the nickel grain 23 (metal ball) about 10 micrometers in diameter is arranged in the slot 12.
[0116]Next, as shown in drawing 7 (b), by heat treatment, the silicone film 22 and the nickel grain 23 are made to react, and the nickel silicide film 24 as a penetration plug is formed in the slot 12. Here, since there are no silicone film 22 and nickel grain 23 of quantity sufficient in the slot 12, a cavity part remains in the upper part of the nickel silicide film 24.
[0117]As finally shown in drawing 7 (c), after depositing the insulator layer or metal membrane used as the cap film 25 on the whole surface, this insulator layer or metal membrane is ground, and the

cavity part of the upper part of the nickel silicide film 24 is filled up with the cap film 25.
[0118]the method (a CVD method.) which had described the method of forming a penetration plug so far Various methods, such as not the thing limited to a sputtering technique, plating, the method using conductive paste, the method using metal particles, the method using a metal ball, and the method using suspension but a method which combined these methods suitably, are possible.
[0119](A 3rd embodiment) Drawing 8 is a sectional view of the multichip semiconductor device concerning a 3rd embodiment of this invention. Drawing 9 is a top view of the connection substrate of the multichip semiconductor device of drawing 8.
[0120]There is the feature of this multichip semiconductor device in having electrically connected mutually two chips of the adjacent upper and lower sides via the connection substrate which has a penetration plug and a heater.
[0121]That is, it connected with the penetration plug 4 of connection substrate 31_1 via the solder bump 8, and the pad 6 provided in the multilayer interconnection layer 3 of chip 1_1 has connected the penetration plug 4 of this connection substrate 31_1 to the penetration plug 4 of chip 1_2 via the solder bump 8.
[0122]Thus, two chip 1_1 of the adjacent upper and lower sides and 1_2 will electrically be mutually connected via the penetration plug 4 of connection substrate 31_1 provided between them. Similarly, chip 1_2 will electrically be connected with chip 1_3 via the penetration plug 4 of connection substrate 31_2. The formation method of the penetration plug 4 applies to it of a 2nd embodiment correspondingly.
[0123]Connection substrate 31_1 and 31_2 are formed so that thermal conductivity may become high enough rather than chip $1_1 - 1_3$.
[0124]Specifically, the component of connection substrate 31_1 and 31_2 is formed of insulating materials, such as the material whose thermal conductivity is higher than the silicon which is a component of the silicon substrate 2, for example, SiC, and SiN. The thing in case the component of connection substrate 31_2 is an insulating material is shown in the figure. For this reason, the insulator layer is not formed in the side of a breakthrough in which the penetration plug 4 was embedded.
[0125]To the inside of a connection substrate main part (penetration plug 4+ connection substrate 31_1, penetration plug 4+ connection substrate 31_2), the metal plate 32 whose thermal conductivity is higher than it is embedded. The components of this metal plate 32 are metal, such as W and Cu, for example. The metal plate 32 may be formed in the surface of connection substrate 31_1 and 31_2, and may be provided in both an inside and the surface.
[0126]The heater 33 embeds and is formed in the surface and the rear face of connection substrate 31_1 and 31_2 so that the solder bump's 8 periphery may be surrounded, respectively. The heater 33 is connected to the external power via the power source line 34 which consists of W etc. which were provided in connection substrate 31_1 and 31_2.
[0127]Each power source line 34 is independently controllable, The heater 33 by which embedding formation was carried out, respectively, i.e., four heaters, can be independently controlled now, respectively at the surface and the rear face of the heater 33 by which embedding formation was carried out by this at the surface and the rear face of connection substrate 31_1, respectively, and connection substrate 31_2. The power source line 34 constitutes a capacitor and supply of the stable power supply is possible for it.
[0128]35 show a wiring board among a figure and 36 shows the multilayer interconnection layer.

Although 31_3 shows the same connection substrate as connection substrate 31_1 and 31_2, it is not used for connection of chips. Although this connection substrate 31_3 is used as a heat sink, it is not necessarily required. The insulator layer of the breakthrough side attachment wall of a semiconductor substrate is omitted.

[0129]In this embodiment, connection substrate 31_1 and 31_2 from thermal conductivity being sufficiently higher than chip $1_1 - 1_3$. Even if chip $1_1 - 1_3$ generate heat at the time of operation of chip $1_1 - 1_3$, the heat can be effectively missed outside via connection substrate 31_1 and 31_2. Thereby, degradation of the operating characteristic of chip 1_1 by generation of heat $- 1_3$ and the ephemeralization of chip $1_1 - 1_3$ can be prevented now.

[0130]Only the vamp linked to the chip according to this embodiment provided in connection substrate 31_1 and 31_2, and **** and the independently controllable heater 33 judged that is poor by inspection by what is fused selectively. Since only a poor chip is selectively separable from a connection substrate, a chip can be repaired easily.

[0131]The situation of repair is shown in drawing 10. Although only the reference number required for explanation is given to the figure, the composition of a multichip semiconductor device is the same as what was shown in drawing 8 (also setting to other embodiments the same).

[0132]Drawing 10 (a) shows signs that the chip is inspected with the inspecting probe, and drawing 10 (b) shows signs that chip 1_2 judged that is poor by inspection, and connection substrate 31_2 connected to it are removed. Chip 1_2 and connection substrate 31_1 connected to it may be removed at the process of drawing 10 (b).

[0133]Then, connection substrate 31_2 to chip 1_2 is separated, and a new chip is connected to connection substrate 31_2. Next, connection substrate 31_2 to which this new chip was connected is connected as before. Then, a chip is inspected, if it is success, repair will be ended, but in being a rejection, it repeats the above-mentioned step until it is passing.

[0134]Although the heater 33 was formed so that the solder bump's 8 periphery might be surrounded, and the case where the solder bump's 8 periphery was heated preferentially was explained by this embodiment, even when the heater 33 is formed so that the whole connection substrate may be heated, repair can be easily performed rather than before.

[0135](A 4th embodiment) Drawing 11 is a sectional view of the multichip semiconductor device concerning a 4th embodiment of this invention.

[0136]There is a point that this embodiment differs from a 3rd embodiment in having formed the radiation fin 37 in connection substrate $31_1 - 31_3$. This radiation fin 37 is fixed to connection substrate $31_1 - 31_3$, for example by adhesives. Other fixing methods, such as fixing, may be used by carrying out metallizing.

[0137]Since it not only misses heat from connection substrate $31_1 - 31_3$, but ****** which misses heat also from the radiation fin 37 whose thermal conductivity is higher than it is made according to this embodiment, heat can be more effectively missed from chip $1_1 - 1_3$.

[0138](A 5th embodiment) Drawing 12 is a sectional view of the multichip semiconductor device concerning a 5th embodiment of this invention.

[0139]There is a point that this embodiment differs from a 4th embodiment in having formed the radiation fin 37 only in the large chip of calorific value. Here, chip 1_2 and 1_3 suppose that calorific value is larger than chip 1_1. In this case, it becomes unnecessary to provide connection substrate 31_3 as a heat sink in chip 1_3, and minuteness making of a device can be attained about a laminating direction.

[0140](A 6th embodiment) Drawing 13 is a sectional view of the multichip semiconductor device concerning a 6th embodiment of this invention.
[0141]The point that this embodiment differs from a 3rd embodiment multilevel-interconnection-izes the inside of connection substrate 31_2, and there is in having carried out the rearrangement of the wiring. The solder bump 8a connected with the upper left solder bump 8c via the plug 38a, the wiring layer 39a, and the plug 38b, and, specifically, is connecting 8 d of solder bumps to the wiring layer 39b via the plug 38c, without connecting with the solder bump 6c on it, without connecting with the solder bump 8b on it.
[0142]Although the heater 33 is embedded and formed in the surface and the rear face of chip 1_3 and it is provided in the position which is separated from the wiring layers 39a and 39b, the heater 33 may be formed in the inside of chip 1_3, and it may provide in the same layer as the wiring layers 39a and 39b.
[0143](A 7th embodiment) Drawing 14 is a sectional view of the multichip semiconductor device concerning a 7th embodiment of this invention.
[0144]The point that this embodiment differs from a 3rd embodiment forms a capacitor in the inside of a connection substrate, and is shown in having attained stabilization of the power supply supplied to a chip. Explanation of connection substrate 31_3 will form the power source wire 40 and the ground line 41 in connection substrate 31_3 so that the ground line 41 may exist in the upper and lower sides of the power source wire 40. Thereby, two capacitors by which direct continuation was carried out are formed in a sliding direction.
[0145]The component of connection substrate 31_3 is an insulating material. 42 and 43 show wiring among the figure. These pads are omitted although the wiring 42 and 43 is connected to a vamp via a pad, respectively. The same capacitor is formed about other connection substrates (un-illustrating) other than connection substrate 31_3.
[0146](An 8th embodiment) Drawing 15 is a sectional view of the multichip semiconductor device concerning an 8th embodiment of this invention.
[0147]The multichip semiconductor device of this embodiment has composition connected to lower layer Si chip 51_2 and 51_3 by laminated wiring board 52_1 in which the upper Si chip 51_1 was formed by Si, and 52_2. 50 show the element formation side of Si chip 51_1 - 51_3 among the figure.
[0148]The pad 53 provided in Si chip 51_1 is connected to the pad 55 provided in laminated wiring board 52_1 via the solder bump 54. This pad 55 via the wiring layer which was formed in laminated wiring board 52_1 and which is not illustrated, the penetration plug 4 linked to this wiring layer, the pad 56 provided in laminated wiring board 52_1, and the solder bump 57, It has connected with the pad 58 provided in laminated wiring board 52_2. Here, the penetration plug 4 and the above-mentioned wiring layer are good [in order to fully demonstrate the original purpose, metal, such as Cu and aluminum, is usually used, but] to put emphasis on making a coefficient of thermal expansion the same to use what was formed with the Si film of high impurity concentration.
[0149]The pad 58 is connected to the wiring layer which was formed in laminated wiring board 52_2 and which is not illustrated, the pad 59 linked to this wiring layer, and the pad 61 provided in Si chip 51_2 and 51_3 via the solder bump 60. The above-mentioned wiring layer uses a metallic material or the Si film of high impurity concentration, as mentioned above.
[0150]Thus, the upper Si chip 51_1 is connected to lower layer Si chip 51_2 and 51_3 via laminated wiring board 52_1 and 52_2.
[0151]Laminated wiring board 52_1 is connected to laminated wiring board 52_2 via the pad 56, the

solder bump 57, and the pad 58. Laminated wiring board 52_2 is similarly connected to the plastic plate 65 via the pad 62, the solder bump 63, and the pad 64. The pad 66 and the solder bump 67 are formed in the plastic plate 65, and the wiring layer 68 which connects between the pads 64 and 66 is formed into the plastic plate 65.

[0152]Between each of Si chip 51_2, and 51_3 and laminated wiring board 52_2, it fills up with the adhesives 69 with which the filler is not mixed between Si chip 51_1 and laminated wiring board 52_1.

[0153]Even if the filler is not mixed in the adhesives 69, the component of Si chip 51_1 - 51_3 and it of laminated wiring board 52_1 and 52_2 are the same Si, Therefore, since the coefficient of thermal expansion of Si chip 51_1 - 51_3 and it of laminated wiring board 52_1 and 52_2 become equal, reliable connection can be obtained.

[0154]On the other hand, since a component differs between laminated wiring board 52_2 and the plastic plate 65 mutually, it fills up with the adhesives 70 with which the filler was mixed between laminated wiring board 52_2 and the plastic plate 65.

The reliability of these 52_2 and connection between 65 is secured.

[0155]Here, since the element is not formed in laminated wiring board 52_1 and 52_2, the pitch between the solder bumps 63 can be set as a desired value. Therefore, the pitch between the solder bumps 63 can be taken to such an extent that the adhesives 70 enter certainly between the solder bumps 63.

[0156]Since laminated wiring board 52_1, 52_2 and Si chip 51_1 - 51_3 are formed by the same Si in the embodiment as stated above, heat distortion is hardly produced in the solder bumps 54 and 60.

[0157]Therefore, high integration of Si chip 51_1 - 51_3 progresses further, Even if the distance between the distance between Si chip 51_1 and laminated wiring board 52_1, Si chip 51_2, and 51_3 and laminated wiring board 52_2 becomes short, The reliability of connection between these is secured, therefore can secure now the reliability of connection between the upper Si chip 51_1, and lower layer Si chip 51_2 and 51_3.

[0158]Since laminated wiring board 52_1, 52_2 and Si chip 51_1 - 51_3 are formed by the same Si, the adhesives 69 in which it is not necessary to bring these coefficients of thermal expansion close to which, therefore the filler is not contained can be used.

[0159]Therefore, high integration of Si chip 51_1 - 51_3 progresses further, Even if the distance between the distance between Si chip 51_1 and laminated wiring board 52_1, Si chip 51_2, and 51_3 and laminated wiring board 52_2 becomes short, Since the portion with which the adhesives 69 are not filled up is not produced, the reliability of connection between the upper Si chip 51_1, and lower layer Si chip 51_2 and 51_3 can be secured.

[0160]Flat-surface area of a device can be made small for the same reason as a 1st embodiment.

[0161]In this embodiment, since it is not necessary to form a penetration plug in Si chip 51_1 in which the element was formed - 51_3, the rise of cost can be controlled. Of course, Si chip 51_1, and Si chip 51_2 and 51_3 may be made the composition connected only via laminated wiring board 52_1 using Si chip 51_1 which has a penetration plug - 51_3.

[0162]Drawing 16 - drawing 18 are the process sectional views showing the manufacturing method of the multichip semiconductor device of this embodiment.

[0163]First, as shown in drawing 16 (a), Si chip 51 $_1$ is created, accumulation formation of the element which is not illustrated to the element formation side 50 of a Si substrate is carried out, then the pad 53 is formed, and the solder bump 54 is continuously formed on the pad 53.
[0164]Next, as shown in drawing 16 (b), the penetration plug 4 and wiring layer which become a Si substrate from Si, and the pad 55 are formed, and laminated wiring board 52 $_1$ is created. The pad 55 is formed in the position corresponding to the pad 33. The pads 33 and 55 are the squares whose one side is 20 micrometers, and the pitch of the pads 33 and 55 is 30 micrometers (the distance between pads is 10 micrometers).
[0165]Next, as shown in drawing 16 (c), alignment of the solder bump 54 of Si chip 51 $_1$ and the pad 55 of laminated wiring board 52 $_1$ is performed, By being filled up with the adhesives 69 of an epoxy system with which the filler is not mixed between Si chip 51 $_1$ and laminated wiring board 52 $_1$ after joining these [54 and 55], Si chip 51 $_1$ forms unit 71 $_1$ which comes to carry out flip chip bonding on laminated wiring board 52 $_1$.
[0166]The distance of the Si substrate which constitutes laminated wiring board 52 $_1$, and the Si substrate which constitutes Si chip 51 $_1$ shall be 20 micrometers. For that purpose, a 20 micrometerphi grade may be sufficient as the size of the solder bump 54.
[0167]Next, as shown in drawing 17 (d), Si chip 51 $_2$ is created, accumulation formation of the element which is not illustrated to the element formation side 50 of a Si substrate is carried out, then the pad 61 is formed, and the solder bump 60 is continuously formed on the pad 61 of Si chip 51 $_2$. Next, as shown in the figure (d), Si chip 51 $_2$ is created similarly, and the solder bump 60 is continuously formed on the pad 61 of Si chip 51 $_2$.
[0168]Next, as shown in drawing 17 (e), the penetration plug 4 and wiring layer, and the pads 58, 59, and 62 which become a Si substrate from Si are formed, laminated wiring board 52 $_2$ is created and then the solder bump 57 is formed on the pad 58.
[0169]Next, as shown in drawing 17 (f), like the case of unit 71 $_1$, Alignment, junction, and restoration of the adhesives 69 are performed and Si chip 51 $_2$ and unit 71 $_2$ to which it comes to carry out flip chip bonding of the 51 $_3$ are formed on laminated wiring board 52 $_2$.
[0170]Next, as shown in drawing 18 (g), unit 71 $_1$ and unit 71 $_2$ are connected by joining the solder bump 58 and the pad 56.
[0171]Since laminated wiring board 52 $_1$, 52 $_2$, Si chip 51 $_2$ - 51 $_3$ are formed by Si at this time, there is no heat distortion by the difference in a coefficient of thermal expansion. Therefore, the heat distortion by the difference in a coefficient of thermal expansion should just perform the size of each vamp, and the design of a pitch only in consideration of the thickness of laminated wiring board 52 $_1$, Si chip 51 $_2$ between 52 $_2$, and 51 $_3$, without taking into consideration.
[0172]Since it is connected with the solder bump 63 of the plastic plate 65, the pad 62 formed in the undersurface of laminated wiring board 52 $_2$ needs to take 100 micrometers of the diameters and pitches of the pad 62, respectively. [not less than about 200 micrometers of] The wiring layer for easing a pitch is formed in laminated wiring board 52 $_2$.
[0173]Finally, as shown in drawing 18 (h), form the plastic plate 65 which has the pads 64 and 66 and the wiring layer 68, then, form the solder bumps 63 and 67 on the pad 64 and 66, and then the plastic plate 65, After carrying out alignment of the unit 71 $_2$ to which unit 71 $_1$ was connected and joining, In order to ease distortion between the plastic plate 65 and unit 71 $_2$, it is filled up with the

adhesives 70 containing the filler of SiO_2, and the multichip semiconductor device shown in drawing 15 is completed.

[0174]According to this embodiment, the Si substrate is used as a substrate of laminated wiring board 52_1 and 52_2. Therefore, cheap and homogeneous laminated wiring board 52_1 and 52_2 can be formed with mass production.

[0175]The design rule of the wiring layer formed in laminated wiring board 52_1 and 52_2 is far loose compared with it of the wiring layer formed in Si chip 51_1 and 51_2 (for example, several micrometers order). Therefore, the yield can also obtain about 100%. Since it is not necessary to form elements, such as a MOS transistor and a capacitor, there is almost no necessity of taking contamination of a Si substrate into consideration, and a process can also be simplified.

[0176]Although this embodiment explained the case where the component of a laminated wiring board was the same as the component of a chip, as long as a coefficient of thermal expansion is almost equal, components may differ. The combination of the component to which the heat dissipation nature of a laminated wiring board (connection substrate) becomes high is better than a chip so that he may like to explain by the paragraph of an operation in this case.

[0177]In the case of the same component, it is good to form a penetration plug, for example with the material whose heat dissipation nature is higher than the component of a laminated wiring board by providing the radiation means of a radiation fin etc. in a laminated wiring board, or giving a radiating function to it at the penetration plug formed in a laminated wiring board. If it is a case where the component of a chip and a laminated wiring board is Si, specifically, it turns out that what is necessary is just to use SiC and AlN from Table 1.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The sectional view of the multichip semiconductor device concerning a 1st embodiment of this invention
[Drawing 2]The process sectional view showing the formation method in the first half of the penetration plug of the multichip semiconductor device concerning a 2nd embodiment of this invention
[Drawing 3]The process sectional view showing the formation method in the first half of the penetration plug of the multichip semiconductor device concerning a 2nd embodiment of this invention
[Drawing 4]The sectional view showing a penetration plug
[Drawing 5]The process sectional view showing the formation method of a slot
[Drawing 6]The process sectional view showing other formation methods of a penetration plug
[Drawing 7]The process sectional view showing another formation method of a penetration plug
[Drawing 8]The sectional view of the multichip semiconductor device concerning a 3rd embodiment of this invention
[Drawing 9]The top view of the connection substrate of the multichip semiconductor device of drawing 8
[Drawing 10]The figure showing the situation of repair of the multichip semiconductor device of drawing 8
[Drawing 11]The sectional view of the multichip semiconductor device concerning a 4th embodiment of this invention
[Drawing 12]The sectional view of the multichip semiconductor device concerning a 5th embodiment of this invention
[Drawing 13]The sectional view of the multichip semiconductor device concerning a 6th embodiment of this invention
[Drawing 14]The sectional view of the multichip semiconductor device concerning a 7th embodiment of this invention
[Drawing 15]The sectional view of the multichip semiconductor device concerning a 7th embodiment of this invention
[Drawing 16]The process sectional view showing the manufacturing method of the multichip semiconductor device of drawing 15
[Drawing 17]The process sectional view showing the manufacturing method of the multichip semiconductor device following drawing 16
[Drawing 18]The process sectional view showing the manufacturing method of the multichip semiconductor device following drawing 17
[Drawing 19]The sectional view of the conventional multichip semiconductor device
[Drawing 20]The sectional view of other conventional multichip semiconductor devices

[Drawing 21]The sectional view of another conventional multichip semiconductor device
[Drawing 22]The sectional view of the multichip semiconductor device using wire bonding as a conventional mounting method
[Drawing 23]The sectional view of the multichip semiconductor device using TAB as a conventional mounting method
[Drawing 24]The sectional view of the multichip semiconductor device using the flip chip as a conventional mounting method
[Description of Notations]
1_1, 1_2, 1_3 -- Chip
2 -- Silicon substrate
3 -- Multilayer interconnection layer
4 -- penetration plug (conductive plug)
4a -- Conductive film
5 -- Insulator layer
6 -- Pad
7 -- Insulator layer
8 -- Solder bump
9 -- Laminated wiring board (connection substrate)
11 -- Mask pattern
12, 12_1 - 12_3 -- Slot
13 -- Low stress film
14 -- Cap metal membrane
15 -- Cap insulation film
16 -- Metal ball
17 -- Metal silicide film
18 -- Conductive paste
19 -- Metal particles
20 -- Silicone film
21 -- Metal silicide film
22 -- Silicone film
23 -- nickel grain
24 -- nickel silicide film
25 -- Cap film
31_1 - 31_3 -- Connection substrate
32 -- Metal plate (a high temperature conductivity member, conductive plates)
33 -- Heater (exothermic part)
34 -- Power source line
35 -- Wiring board
36 -- Multilayer interconnection layer
37 -- Radiation fin
38a-38c -- Plug
39a, 39b -- Wiring layer
40 -- Power source wire
41 -- Ground line
42, 43 -- Wiring
50 -- Element formation side
51_1, 51_2, 51_3 -- Si chip
52_1, 52_2 -- Laminated wiring board (connection substrate)

53 -- Pad
54 -- Solder bump
55 -- Pad
4 -- Penetration plug
56 -- Pad
57 -- Solder bump
58, 59 -- Pad
60 -- Solder bump
61, 62 -- Pad
63 -- Solder bump
64 -- Pad
65 -- Plastic plate
66 -- Pad
67 -- Solder bump
68 -- Wiring layer
69 -- Adhesives (with no filler)
70 -- Adhesives (with a filler)
71_1, 71_2 -- Unit

[Translation done.]